Raytheon

Miniature Microwave Frequency Multiplexers

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A novel frequency multiplexer has been developed which divides the 6-18 GHz band into 8 equal size sub-bands. The multiplexer consists of seven diplexers, each of which was realized as an individual MMIC. Two prototype multiplexers were assembled and evaluated.

The diplexers take advantage of a novel filter design approach. In this approach, conventional lumped element filters define the basic filter shape. In addition, transversal filter elements are integrated, and serve to sharpen the band edge rejection characteristics. These transversal elements are realized with active mode MESFETs.

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1.0 INTRODUCTION

The goal of this program is to develop an eight-channel miniature frequency multiplexer for the 6-18 GHz band. The multiplexer must be small enough to fit into the narrow 6-18 GHz phase array modules with MMICs. The program is organized into two phases: the first was for component diplexer development, the second is for the complete multiplexer. The goals for each phase are given in Sections 2 and 3, respectively.

Phase I of the program has been successfully completed. Our Phase I work is reviewed in Section 2 of this report. This final report emphasizes the results of our Phase II work which is detailed in Sections 3, 4 and 5.

2.0 PHASE I

The goal of Phase I was to develop an MMIC diplexer that can be used as a miniature multiplexer building block. A lumped and transversal element filter had already been developed, and under this phase that approach was extended to a diplexer.

2.1 Specifications

Table 2-1 lists the diplexer design specifications.

Table 2-1
Diplexer Specifications

Output Band 1	1.5 GHz wide
Output Band 2	1.5 GHz wide
Insertion Loss	0 dB within pass band
Return Loss	10 dB within pass band
Rejection	30 dB 1.5 GHz from output band edges
Skirt Characteristics	Repeatable and well defined
Noise Figure	10.5 dB
1 dB Compressed Power	15 dBm

The 0 dB insertion loss specification cannot be satisfied using lumped element filters when typical lumped element MMIC loss is included. In addition, the 30 dB signal rejection requirement, considered the critical design parameter, is difficult to satisfy using lumped element filters of moderate order.

2.2 Lumped/Transversal Element Filters

A low order, MMIC filter using lumped and transversal elements has been demonstrated. This filter, described in Appendix A, has low pass band loss and high signal rejection near its pass band edges. The use of transversal elements reduced pass band loss and increased the filter rejection out of band. In addition, the filter was of moderate complexity and fabricated as an MMIC. These

qualities merited further study of lumped/transversal filters for use as diplexer building blocks.

2.3 High Pass/High Pass, Low Pass/Low Pass

A diplexer composed of high pass input, high pass output and low pass input, low pass output transversal filters was designed to produce a cut-off band edge at 7.5 GHz and a turn-on band edge at 7.5 GHz. This diplexer would be used in the output stage in a high pass/high pass, low pass/low pass multiplexer configuration. Figure 2-1 shows a schematic of the diplexer with FET peripheries shown in millimeters. The low pass filters were designed to turn-off nominally at 7.5 GHz and the high pass filters were designed to turn-on nominally at 7.5 GHz. Two FETs were used as transversal elements in the high pass/high pass filter and three FETs were used as transversal elements in the low pass/low pass filter.

Figure 2-2 shows the predicted performance of the diplexer. There is gain in both the low pass and high pass bands of the diplexer. The rejection at 9 GHz and at 6 GHz (1.5 GHz from each band edge) is greater than 38 dB. Since this diplexer produces band edges for both the 6-7.5 GHz and 7.5-9 GHz sub-bands, the diplexer must be well matched from 6-9 GHz. The input return loss is greater than 9 dB from 6-9 GHz in a 30 Ω system (since this node is internal to the multiplexer the input does not have to be matched to 50 Ω).

2.4 Band Pass

A second diplexer composed of high pass input, low pass output transversal filters was designed to produce pass bands from 12-13.5 GHz and from 15-16.5 GHz. This diplexer would be used in a band pass multiplexer configuration.

The schematic of the diplexer, with FET peripheries in millimeters, is shown in Figure 2-3. Both filters use three FETs as transversal elements. The predicted performance of the diplexer is shown in Figure 2-4. For the low frequency pass band, there is gain

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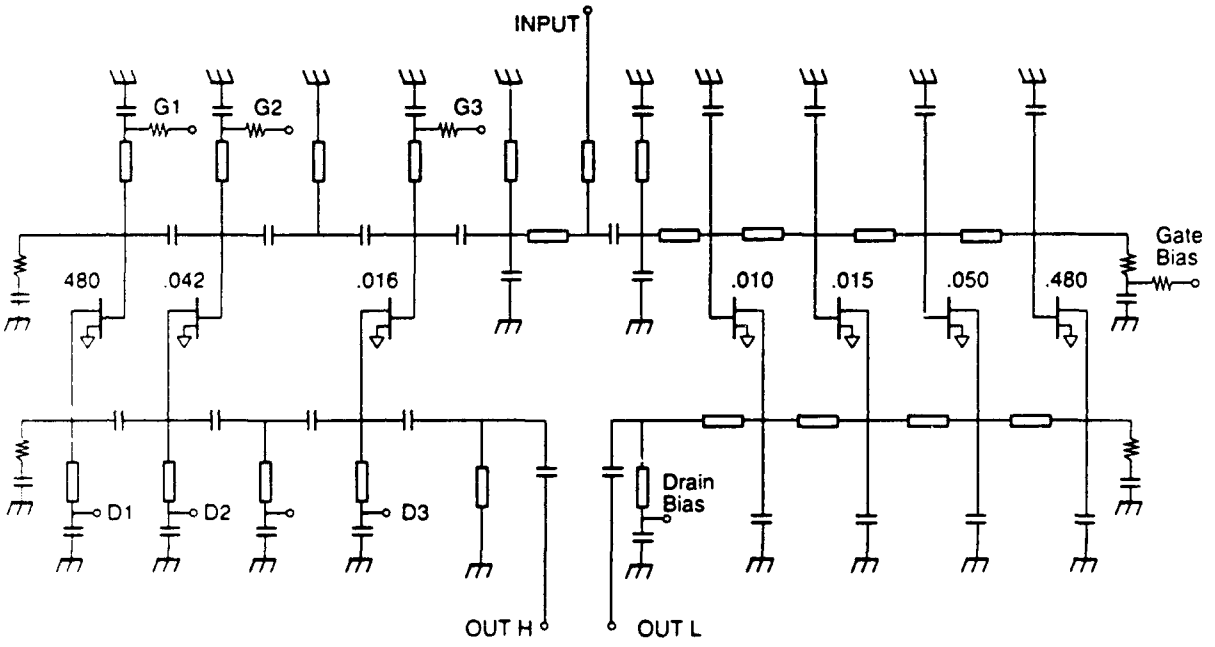

Figure 2-1. High Pass/High Pass, Low Pass/Low Pass Diplexer Schematic.

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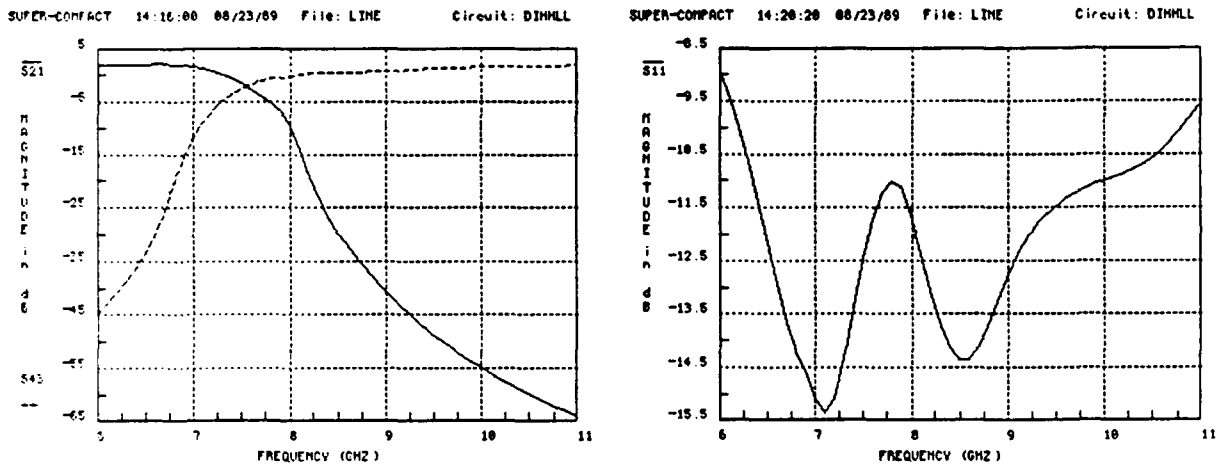

Figure 2-2. High Pass/High Pass, Low Pass/Low Pass Diplexer Predicted Performance.

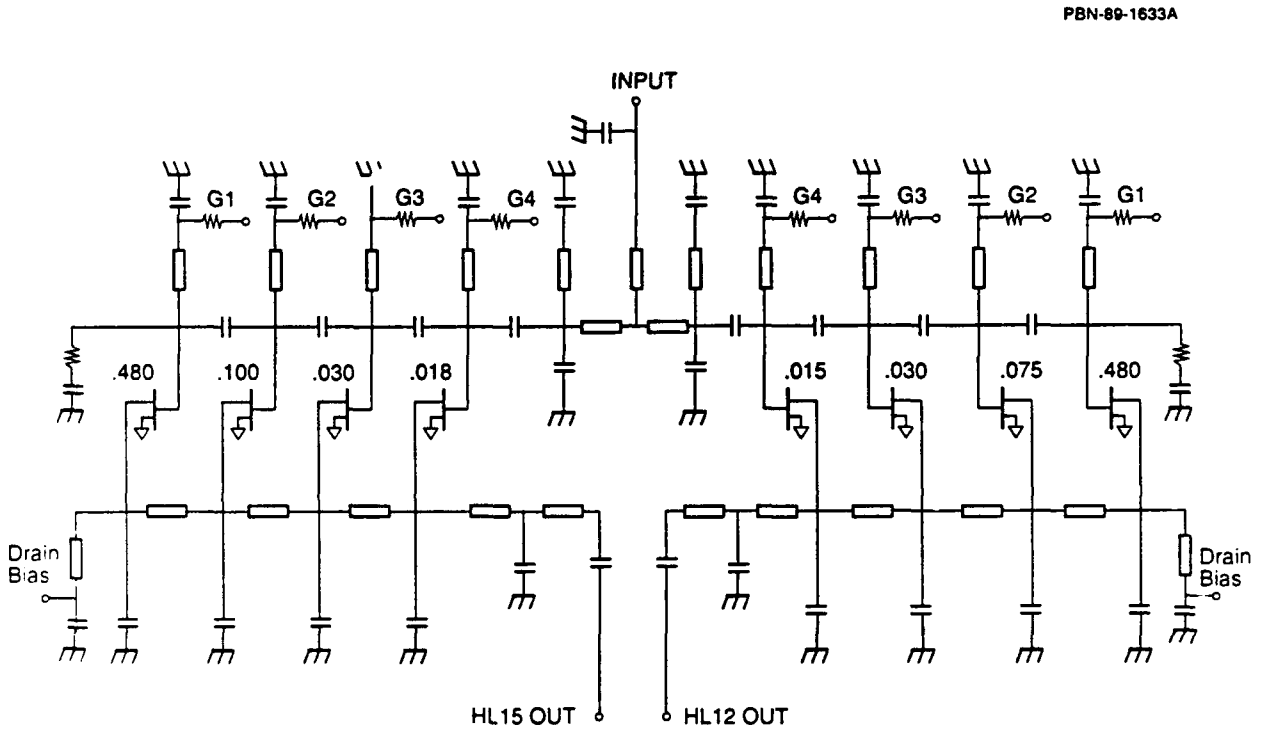

Figure 2-3. Band Pass Diplexer Schematic.

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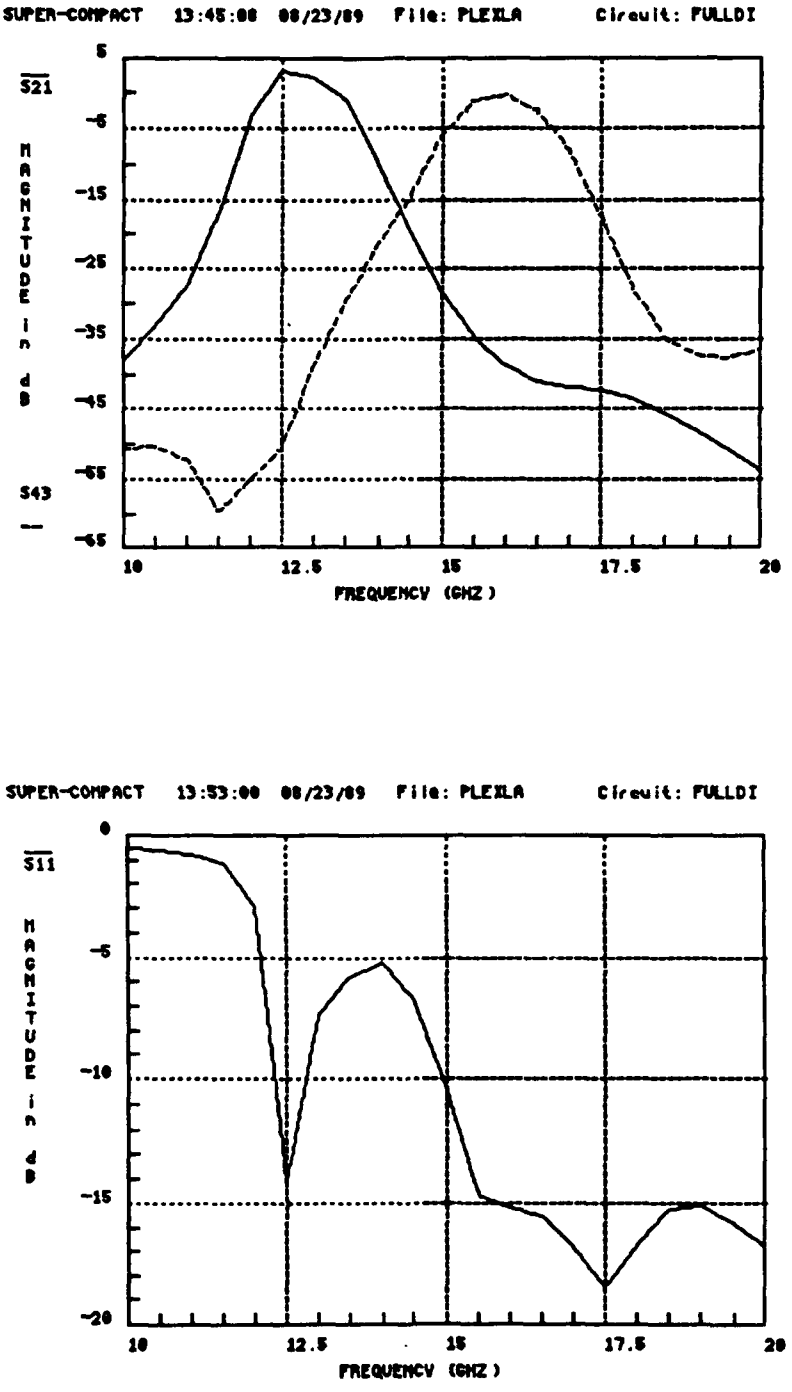

Figure 2-4. Band Pass Predicted Performance.

in the pass band and 30 dB of rejection 1.5 GHz from both band edges. For the high frequency pass band, there is little or no gain in the pass band. The rejection at both band edges is 25 dB. The input return loss of the diplexer is greater than 10 dB in the high frequency band but is less than 10 dB at the edges of the low frequency pass band.

2.5 Processing

Both diplexers were processed as MMICs. The FET active layer was formed by ion implantation with a doping level of 3×10^{17} cm^{-3}. The FET gate length is 0.5 μm. The gates are biased through 2 kΩ resistors and all FET bias circuitry is included on chip. The chips are passivated with 2000 Å of silicon nitride which is also used as the capacitor dielectric. Inductive elements were formed using high impedance transmission lines. Upon completion of front-side processing, the wafer was thinned to 4 mils and 50 μm via holes were etched. Figure 2-5 shows a chip photograph of the high pass/high pass, low pass/low pass diplexer and Figure 2-6 shows a chip photograph of the band pass diplexer. Both diplexers measure 174 x 88 mils (4.4 x 2.2 mm).

2.6 Performance

Figure 2-7 shows the small signal performance of the high pass/high pass, low pass/low pass diplexer designed to turn-on and cut-off at 7.5 GHz. The low pass output has gain (cut-off at 4 GHz due to series blocking cap) and a sharp cut-off characteristic. At 7.5 GHz, there is 0.7 dB of loss. At 9 GHz (1.5 GHz from the band edge), there is greater than 31 dB of signal rejection relative to the band edge. The high pass output is shifted high in frequency by 1.5 GHz. This frequency shift is due to incorrect high pass filter series capacitor values. The high pass output has gain at 9 GHz (shifted band edge); there is 0.8 dB of loss. At 7.5 GHz (assuming 9 GHz turn-on frequency), there is greater than 31 dB of rejection relative to the band edge. The input return loss is between 7 and 20 dB from 4-11 GHz when measured in a 50 Ω system. The input

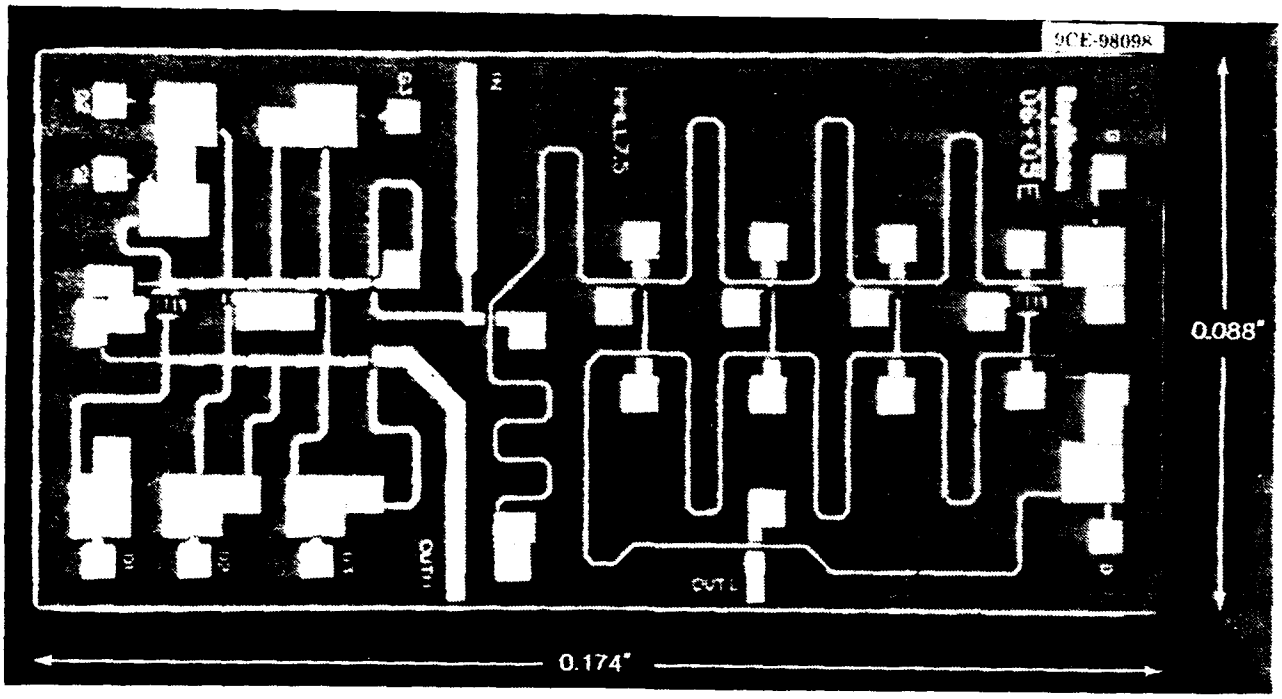

Figure 2-5. High Pass/High Pass Diplexer Chip Photograph.

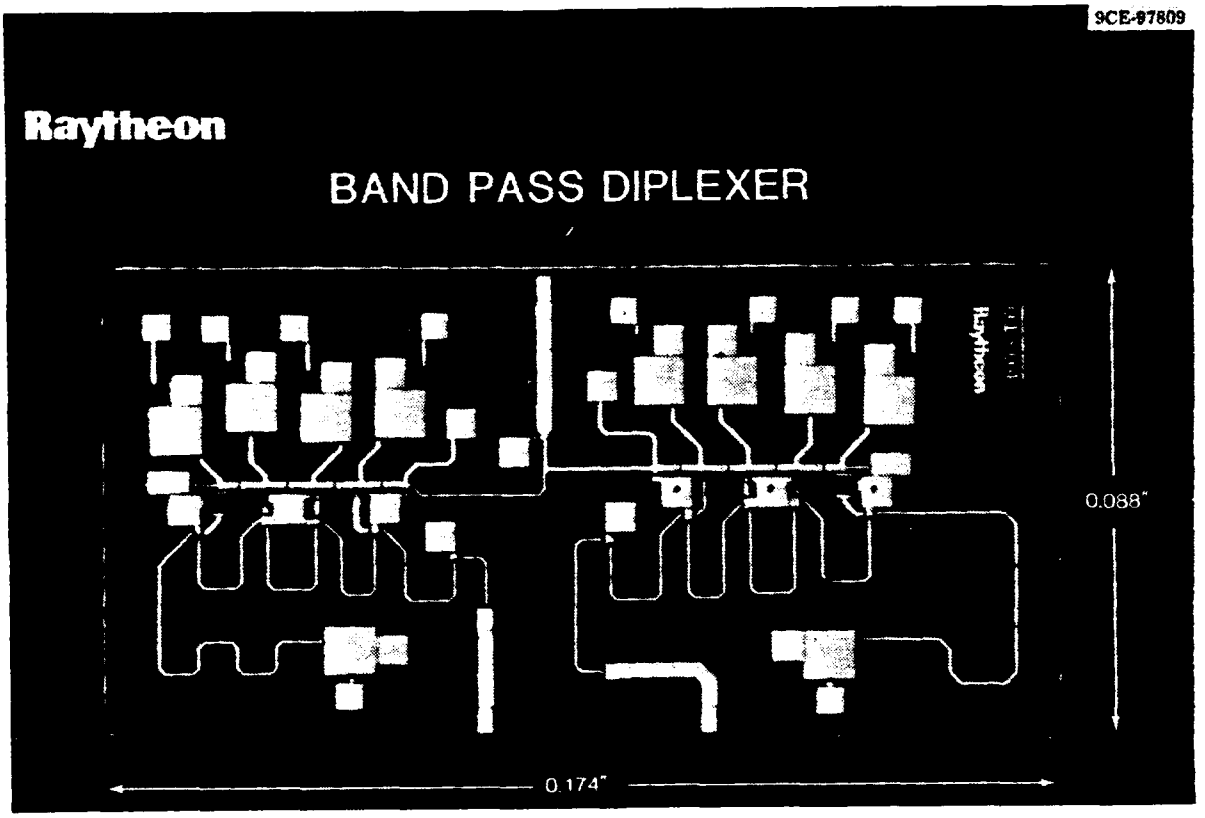

Figure 2-6. Band Pass Diplexer Chip Photograph.

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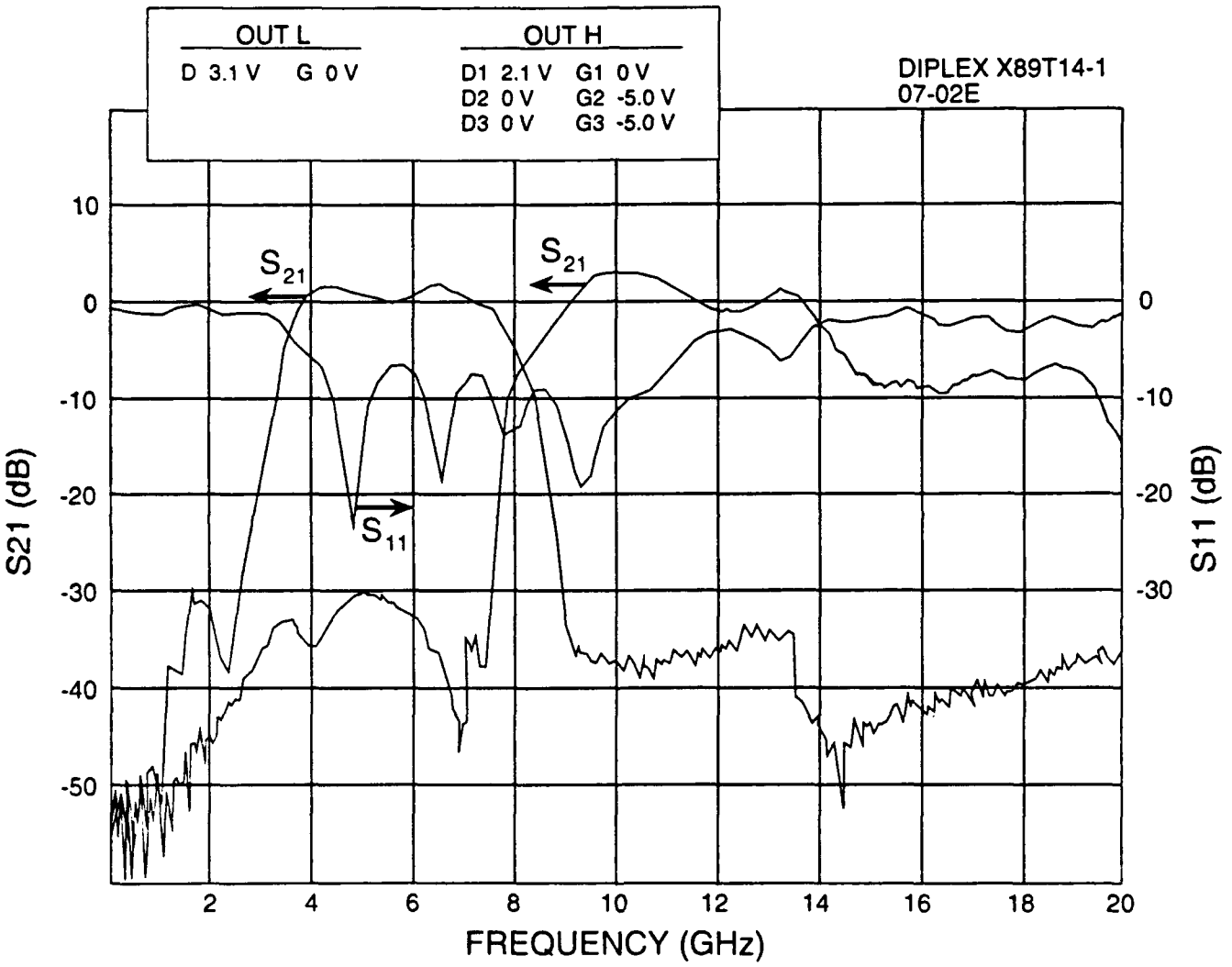

Figure 2-7. High Pass/High Pass, Low Pass/Low Pass Diplexer Measured Performance.

return loss would be higher if measured in a 30 Ω input impedance system (designed to operate in a 30 Ω system).

The small signal performance of the band pass diplexer is shown in Figure 2-8. Two distinct pass bands are evident. Although neither pass band has gain, both bands have sharp cut-off band edges. The low frequency output, designed to produce a 12-13.5 GHz pass band, has minimum loss at 12.7 GHz. The loss at 12 GHz is 14.3 dB and the loss at 13.5 GHz is 5.7 dB. At 10.5 GHz, the signal rejection is 44 dB relative to 12 GHz. The rejection at 15 GHz is 27 dB relative to 13.5 GHz. The high frequency output, designed to produce a 15-16.5 GHz pass band, has minimum loss at 15.8 GHz. The loss at 15 GHz is 10 dB and the loss at 16.5 GHz is 7.9 dB. The rejection at 13.5 GHz is 29 dB relative to 15 GHz and the rejection at 18 GHz is 33 dB relative to 16.5 GHz. The input return loss is > 7 dB within the low frequency pass band (except at the low band edge) and > 10 dB in the high frequency pass band. The power performance of the diplexer at 13 GHz is shown in Figure 2-9. The output power is 1 dB compressed at an input power of 19.5 dBm (89 mW).

The measured performance of both diplexers is summarized in Table 2-2. Both diplexers have high signal rejection out of band. The high pass/high pass, low pass/low pass diplexer has gain in its pass bands while the band pass diplexer has loss in its pass bands. The power performance of the band pass diplexer satisfies the diplexer power specification and it is expected that the high pass/high pass, low pass/low pass diplexer has similar power performance. Since the high pass/high pass, low pass/low pass diplexer has high signal rejection out of band and gain in its pass bands, it is considered the best diplexer configuration for use as multiplexer building blocks.

Table 2-2
Diplexer Measured Performance Summary

	High Pass/Low Pass Low Pass/High Pass	Band Pass
Signal Rejection	> 31 dB	> 27 dB
Pass Band Gain	> 0 dB	< -3 dB
Input Return Loss	> 7 dB	> 7 dB
1 dB Compressed Power	--	19.5 dBm

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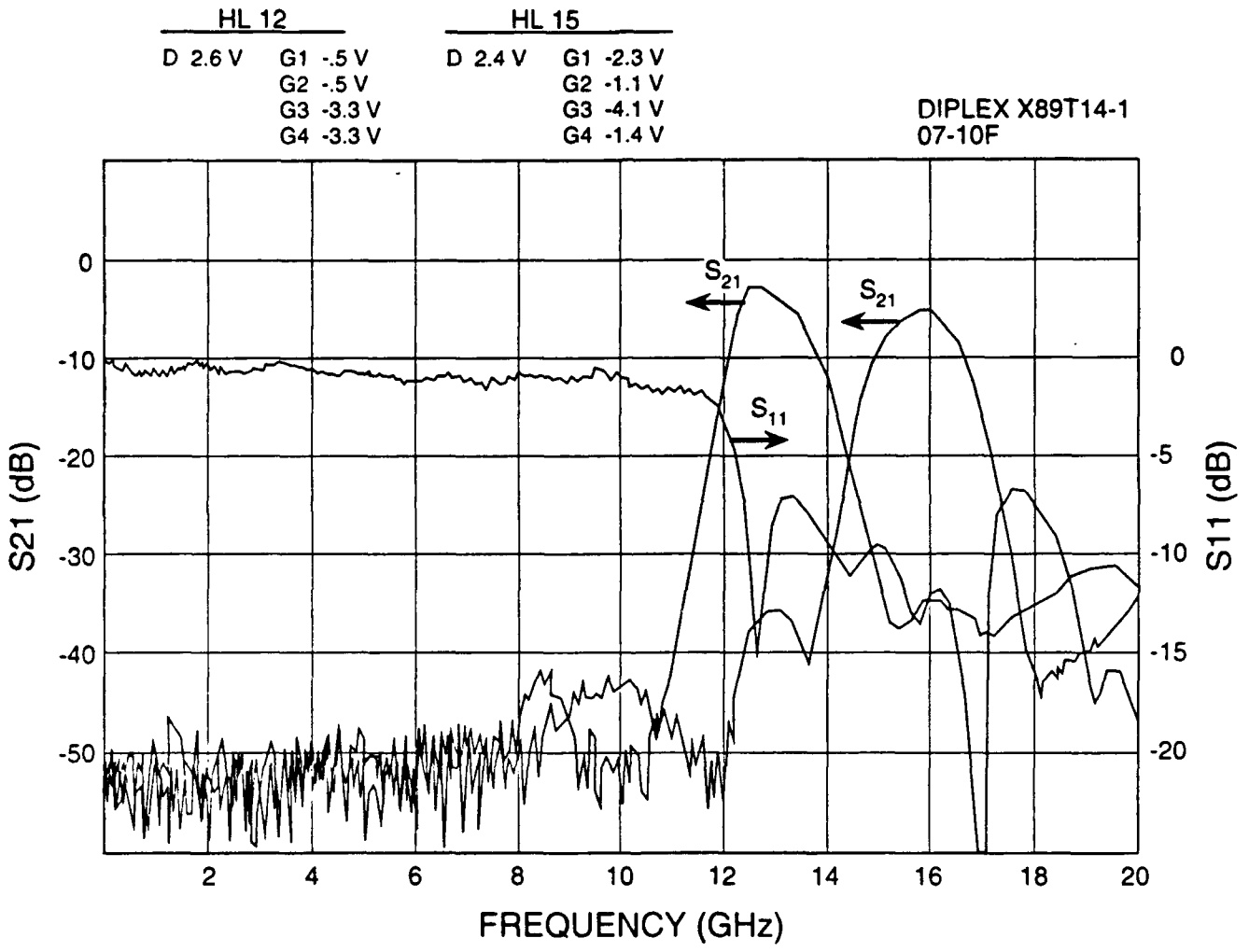

Figure 2-8. Band Pass Diplexer Measured Performance.

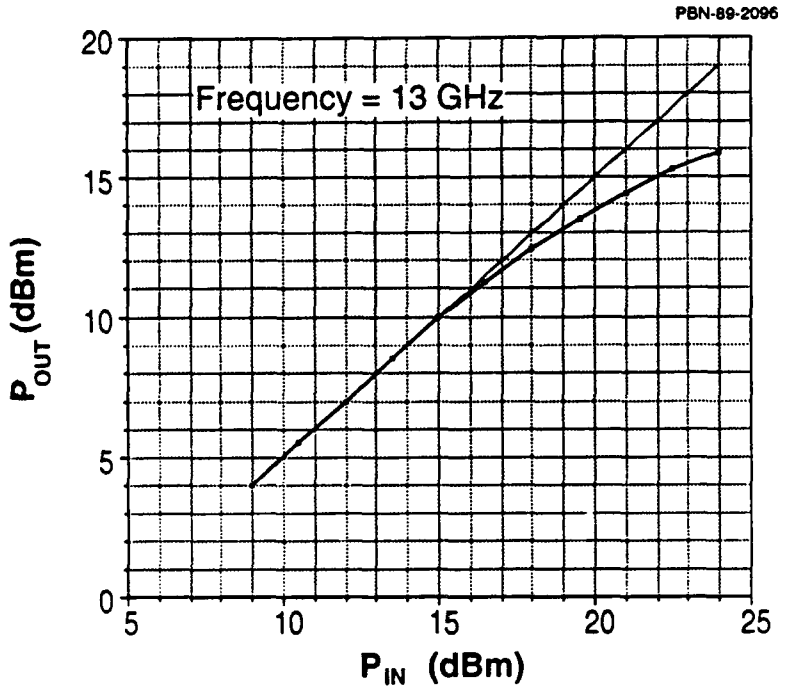

Figure 2-9. Band Pass Diplexer Power Performance.

2.7 Phase I Conclusion

Two wideband microwave multiplexer configurations have been developed. Diplexers were used as building blocks in both multiplexer configurations. In order to obtain low pass band loss and high signal rejection out of band, lumped/transversal element filters were used to form the diplexers.

Two diplexers, one from each multiplexer configuration, were designed and fabricated as MMICs. One diplexer uses high pass input, high pass output and low pass input, low pass output lumped/transversal element filters to form sharp turn-on and cut-off band edges and the second uses high pass input, low pass output lumped/transversal element filters to form band pass outputs.

Both diplexer structures have high signal rejection out of band. The high pass/high pass, low pass/low pass diplexer has gain in its pass bands. The power performance of the band pass diplexer meets the diplexer specification and it is expected that the high pass/high pass, low pass/low pass diplexer has similar power performance.

A diplexer composed of high pass input, high pass output, low pass input, low pass output lumped/transversal filters has been demonstrated that satisfies the Phase I diplexer signal rejection and gain specifications. A multiplexer configured of high pass/high pass, low pass/low pass diplexers does not require splitter circuity. High pass/high pass, low pass/low pass diplexers were selected for use as multiplexer building blocks.

3.0 PHASE II

3.1 Multiplexer Development

The goal of Phase II program is to develop a complete MMIC multiplexer module using the techniques developed in Phase I of the program.

Raytheon's approach is based on novel MMIC active filter structures which incorporate both lumped and transversal elements. The filter structures have been adapted for use as diplexers. The final eight-band multiplexer will be comprised of seven diplexers.

3.2 Specifications

Multiplexer is formed by utilizing seven diplexers. Table 3-1 lists the overall multiplexer design specifications.

Table 3-1
Multiplexer Specifications

Frequency Bands	6-18 GHz input 8 equal output sub-bands
Insertion Loss	0 dB
Input Return Loss	10 dB (in band)
Output Return Loss	10 dB (in sub-band)
Rejection	30 dB (1.5 GHz from sub-band edge)
Skirt Characteristics	Repeatable and well-defined
Noise Figure	12 dB
1 dB Compressed Power	15 dBm

The 0 dB insertion loss specification cannot be satisfied using lumped element filters when typical lumped element MMIC loss is included. In addition, the 30 dB signal rejection requirement, considered the critical design parameter, is difficult to satisfy using lumped element filters of moderate order.

3.3 Multiplexer Design Approach

The configuration chosen for multiplexer is comprised of seven diplexer sections as shown in Figure 3-1. This topology utilizes diplexers which are designed using low pass/low pass high pass/high pass filter sections. Minimum bandpass loss is achieved for each output channel using this approach. The alternative approach of using signal splitters and/or band pass filters would have introduced more loss into the overall multiplexer performance (see Section 2).

The seven diplexers are designed to meet the selectivity requirements indicated in Figure 3-1. Each diplexer is laid out to accommodate the overall multiplexer signal flow and is configured as shown in Figure 3-2. This configuration also satisfies the assembly and measurement requirements of the multiplexer. The use of seven discrete diplexers in the module helps in characterizing each diplexer and evaluating it's contribution to the overall multiplexer module.

The diplexers were laid out for RF probing by providing ground-signal-ground configuration for RF input and RF output pads on each chip. The RF good diplexer chips were then selected for the multiplexer assembly; the need for final frontside dc test was eliminated.

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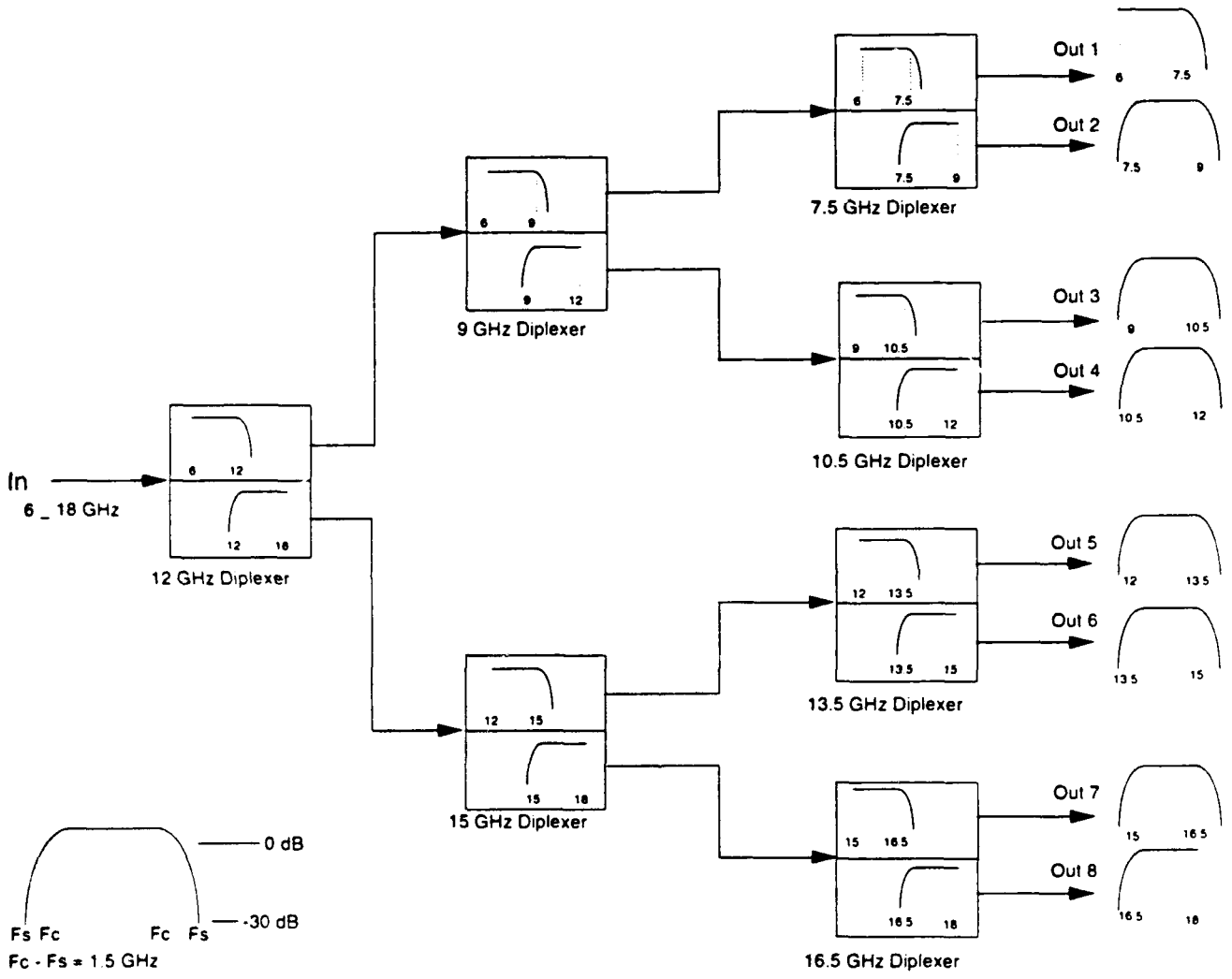

Figure 3-1. Multiplexer Block Diagram and Required Response.

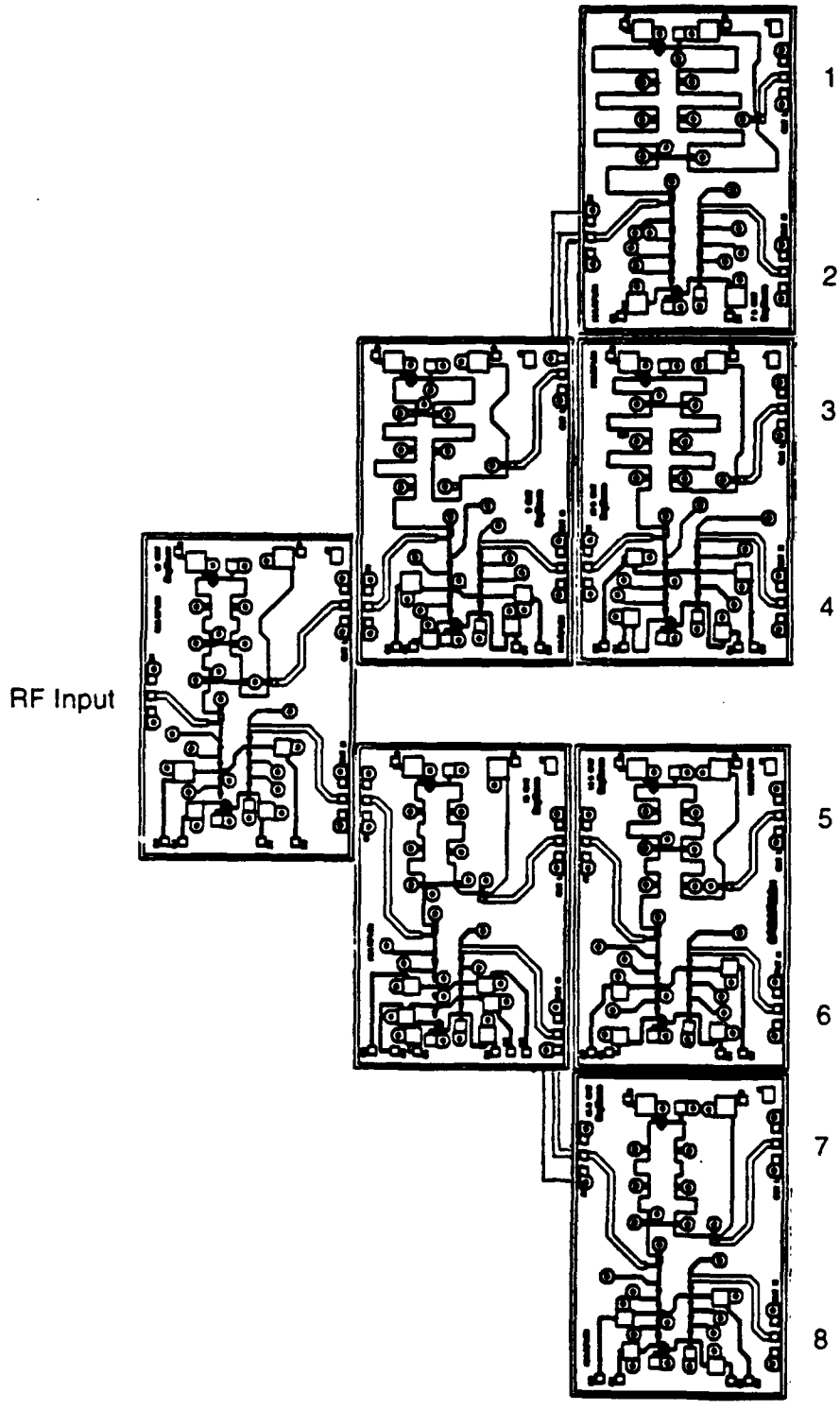

Figure 3-2. Multiplexer Assembly and RF Signal Flow. One RF input, eight channels RF output.

4.0 DIPLEXER DESIGN AND PERFORMANCE

Seven diplexers were designed and characterized as building blocks for the multiplexer module. Each diplexer was designed to meet certain selectivity requirements depending on it's location in the multiplexer module. The performance characteristics are summarized in Table 4-1.

4.1 Lumped/Transversal Filter Structure

Diplexers using lumped/transversal element filters were used to satisfy the selectivity requirements of the multiplexer module. Each diplexer consisted of a high pass and a low pass filter section and each section used two nine-element Chebyshev filters. This filter order gives moderate filter size and complexity. In addition to lumped elements, the filter uses a FET as a cascade element. FETs were also used as transversal elements and are included in all the circuits, except the 7.5 GHz high pass section.

The diplexer design was initiated by taking a basic normalized filter building block and scaling it to different impedance levels. The impedance levels were chosen to provide component sizes that comply with the layout rules and are easily realizable. The final design includes capacitor values between 0.1 and 1.5 pF. Inductors were realized by transmission lines 200 to 1800 μm in length. Figure 4-1 shows the impedance levels selected for each diplexer.

Figure 4-2 shows the block diagram for each diplexer chip and Figure 4-3 is a picture of a typical diplexer. The LOLO CKT in Figure 4-2 refers to the low pass/low pass circuit structure. The HIHI CKT in Figure 4-2 refers to the high pass/high pass circuit structure. Figures 4-4 through 4-27 show the individual circuit diagrams, layouts, predicted performances and measured responses for each diplexer. Figure 4-12 shows the loading effects when a 2-port low pass/low pass and a 2-port high pass/high pass filter form a 3-port diplexer. The contribution of the components to this effect varies from diplexer to diplexer.

TABLE 4-1

Diplexer Performance Summary

Diplexer Module	Predicted Freq. (att.)		Measured Freq. (att.)		Compare to Spec.	
Low Pass Section						
7.5	fc 7.5	(-1.0)	fc 8.0	(-1.0)	+0.5	(-1.0)
	fs 9.0	(-40.0)	fs 9.5	(-40.0)	+0.5	(ok)
9.0	fc 9.0	(-4.5)	fc 10.0	(-6.0)	+1.0	(-6.0)
	fs 10.5	(-40.0)	fs 11.5	(-36.0)	+1.0	(ok)
10.5	fc 10.5	(0.0)	fc 11.5	(-3.0)	+1.0	(-3.0)
	fs 12.0	(-40.0)	fs 13.0	(-39.0)	+1.0	(ok)
12.0	fc 12.0	(2.0)	fc 14.0	(0.0)	+2.0	(ok)
	fs 13.5	(-35.0)	fs 15.5	(-35.0)	+2.0	(ok)
13.5	fc 13.5	(1.0)	fc 14.5	(0.0)	+1.0	(ok)
	fs 15.0	(-40.0)	fs 16.0	(-22.0)	+1.0	(-8.0)
15.0	fc 15.0	(0.0)	fc 16.0	(-3.0)	+1.0	(-3.0)
	fs 16.5	(-35.0)	fs 17.5	(-13.0)	+1.0	(-17.0)
16.5	fc 16.5	(-1.0)	fc 18.0	(-3.0)	+1.5	(-3.0)
	fs 18.0	(-40.0)	fs 19.5	(-20.0)	+1.5	(-10.0)
High Pass Section						
7.5	fc 7.5	(-2.0)	fc 8.0	(-6.0)	+0.5	(-6.0)
	fs 6.0	(-40.0)	fs 6.5	(-39.0)	+0.5	(-9.0)
9.0	fc 9.0	(-2.5)	fc 10.0	(-7.0)	+1.0	(-7.0)
	fs 7.5	(-40.0)	fs 8.5	(-22.0)	+1.0	(-8.0)
10.5	fc 10.5	(-3.0)	fc 11.5	(-5.0)	+1.0	(-5.0)
	fs 9.0	(-36.0)	fs 10.0	(-32.0)	+1.0	(ok)
12.0	fc 12.0	(-2.0)	fc 13.0	(-14.0)	+1.0	(-14.0)
	fs 10.5	(-27.0)	fs 11.5	(-25.0)	+1.0	(-5.0)
13.5	fc 13.5	(2.0)	fc 14.5	(-12.0)	+1.0	(-12.0)
	fs 12.0	(-40.0)	fs 13.0	(-32.0)	+1.0	(ok)
15.0	fc 15.0	(1.0)	fc 16.0	(-12.0)	+1.0	(-12.0)
	fs 13.5	(-36.0)	fs 14.5	(-34.0)	+1.0	(ok)
16.5	fc 16.5	(1.0)	fc 18.0	(-7.0)	+1.5	(-7.0)
	fs 15.0	(-35.0)	fs 16.5	(-25.0)	+1.5	(-5.0)

fc = cutoff frequency, GHz
fs = stopband frequency, GHz
att. = attenuation or gain, dB

Figure 4-13 includes typical input/output return loss response for the 10.5 GHz diplexer. Other diplexers have input/output return loss similar to this in their respective pass-bands. The effects of loading and transmission line couplings are greater in the 12 GHz diplexer, shown in Figure 4-17. There is coupling between the low pass and high pass sections on the chip, contributing to a degradation of the high pass section. Once the low pass section is turned off, the high pass response improves dramatically.

The performance of the diplexers is summarized in Table 4-1. The measured cutoff frequency is 0.5 to 2 GHz higher than the predicted frequency. The measured pass-band gain and stop-band rejection at the measured frequencies is compared to the specifications.

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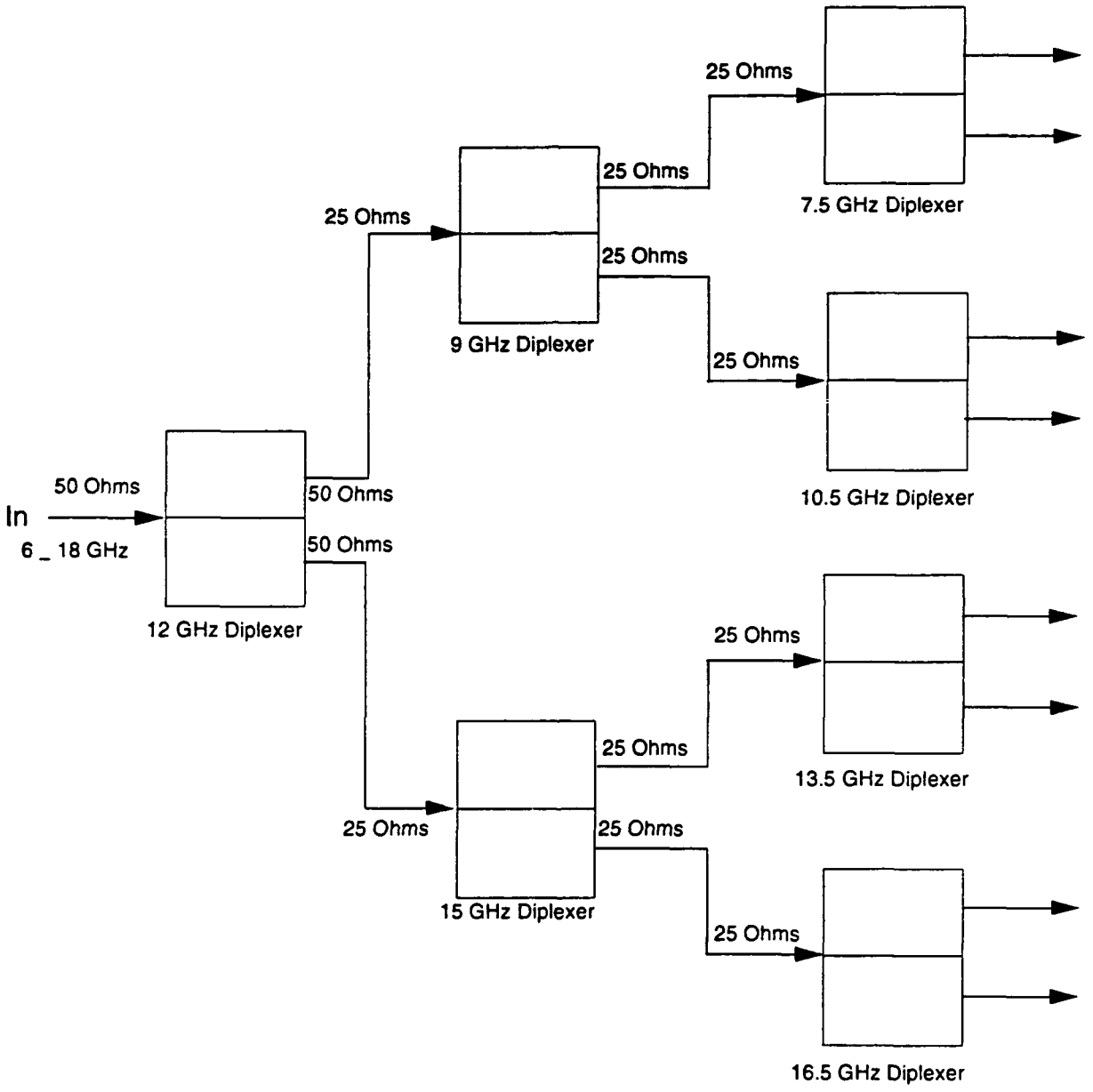


Figure 4-1. Block Diagram of the Multiplexer. All outputs are 50 Ω.

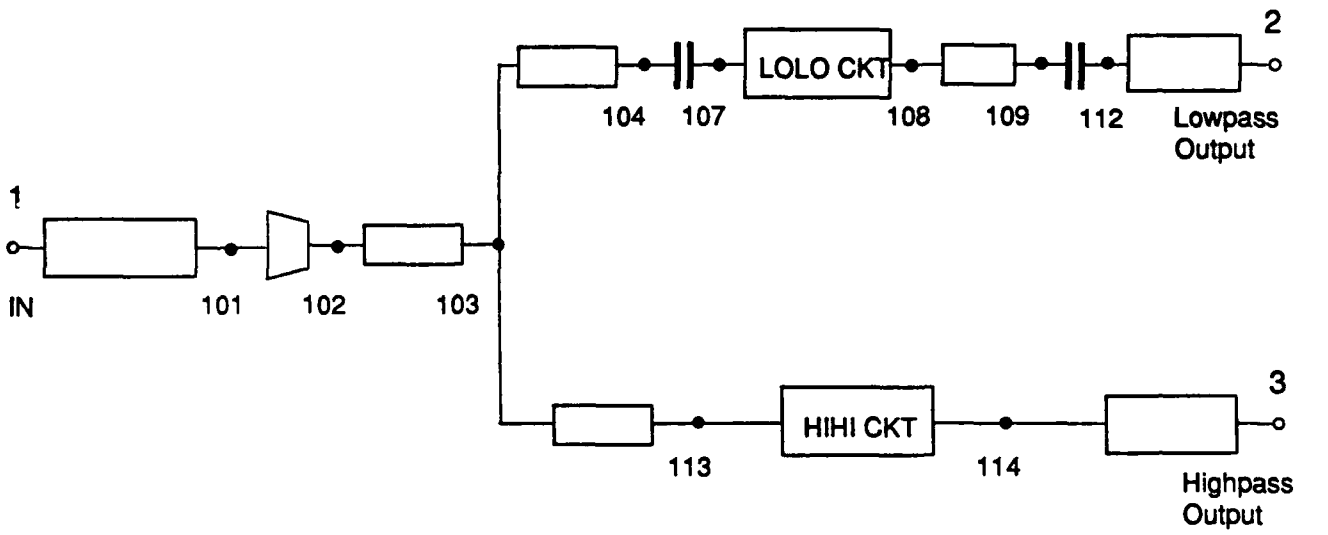


Figure 4-2. Diplexer Block Diagram.

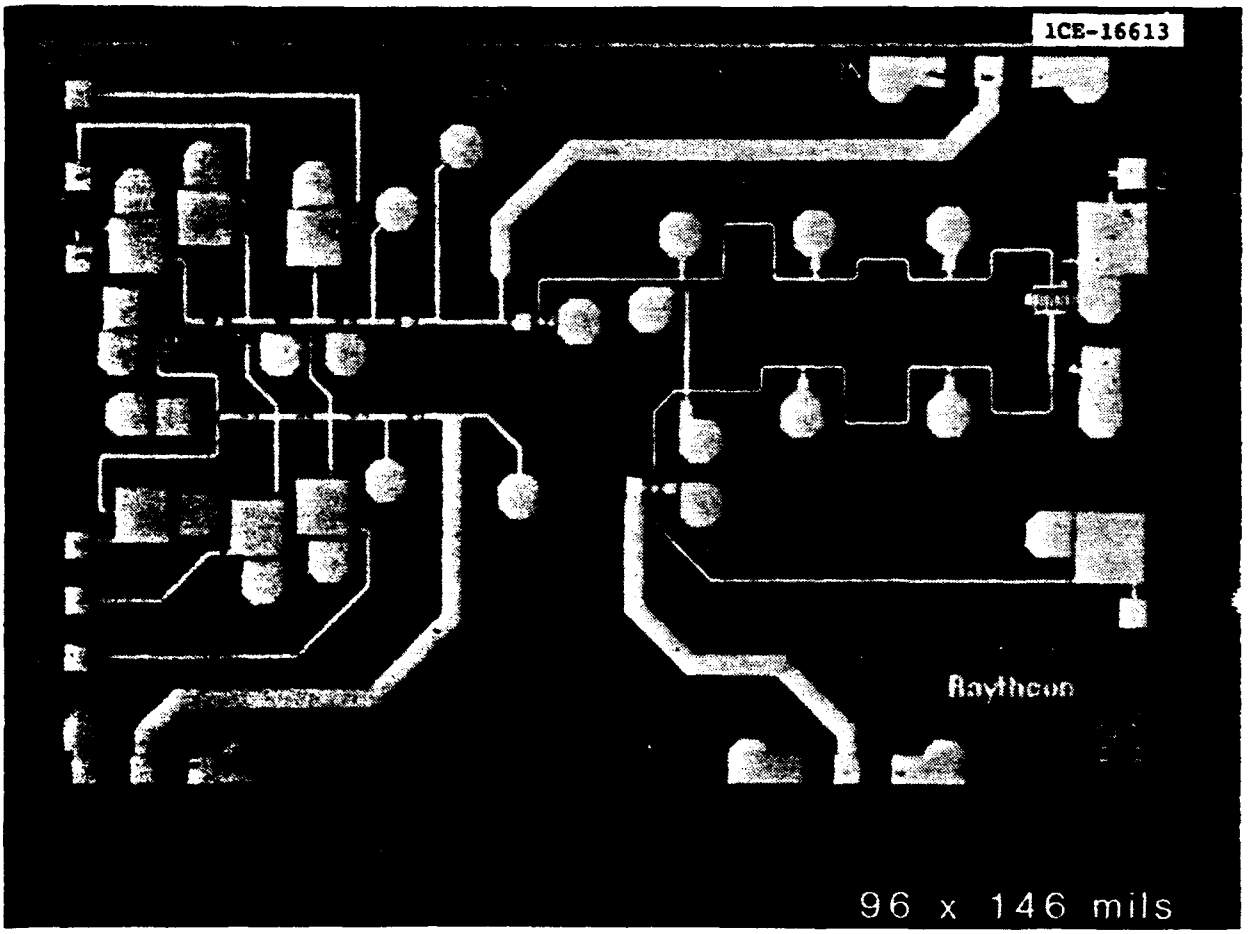
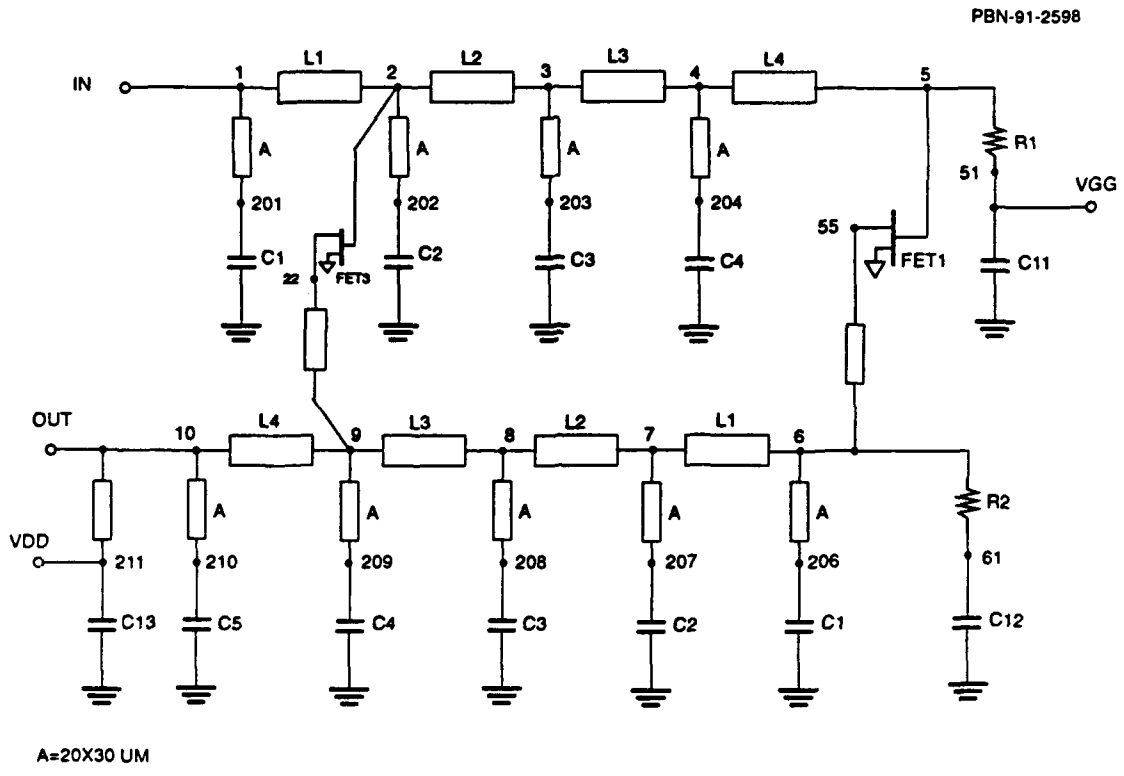


Figure 4-3. A Photograph of the 15 GHz Diplexer Chip.



DIPLEXER LOW PASS SECTION - 7.5 GHZ

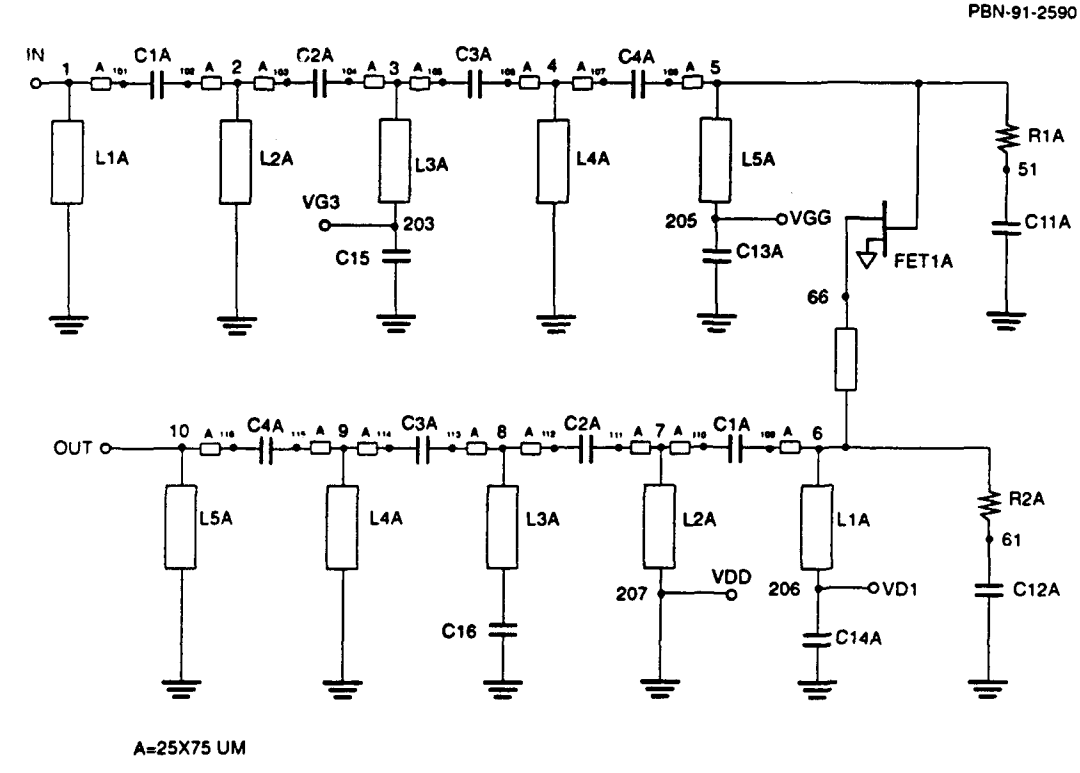


Figure 4-4. Schematic for the 7.5 GHz Diplexer.

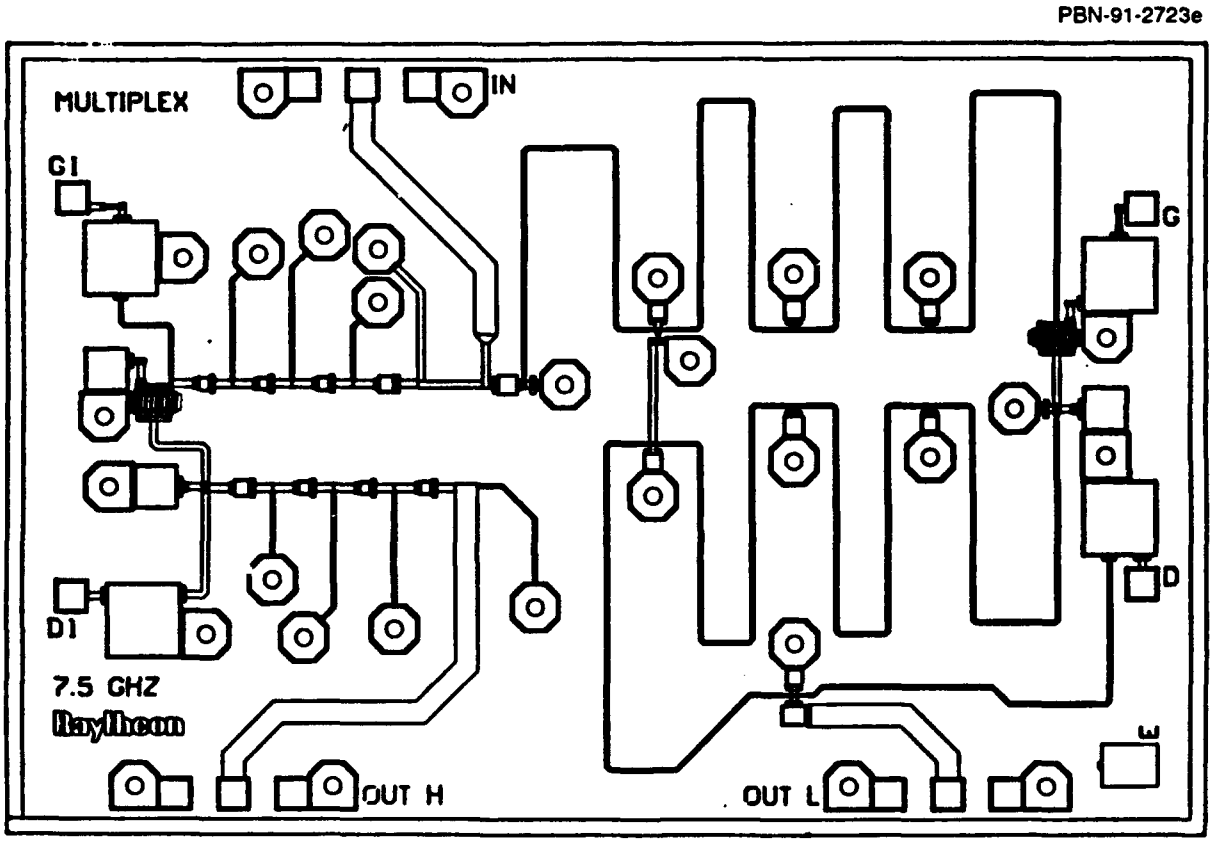


Figure 4-5. Circuit Layout for the 7.5 GHz Diplexer.

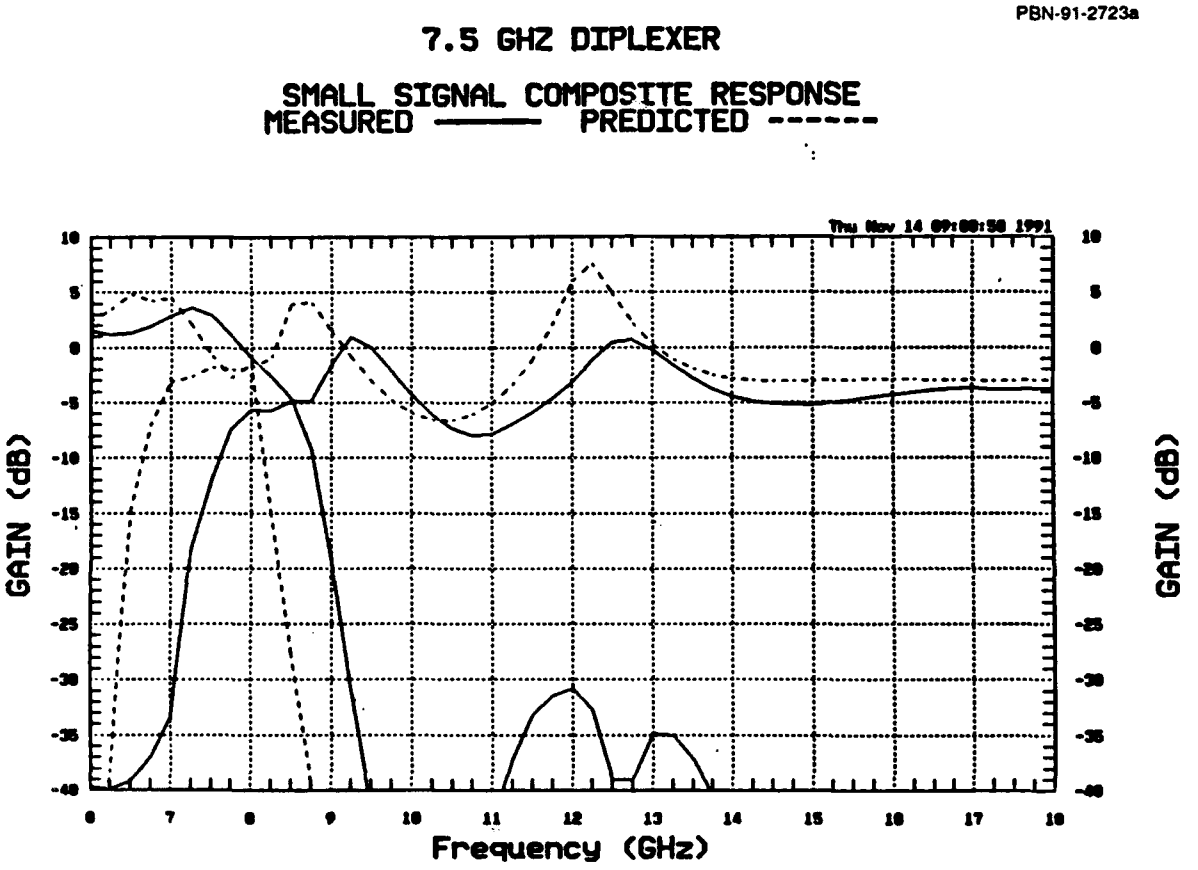
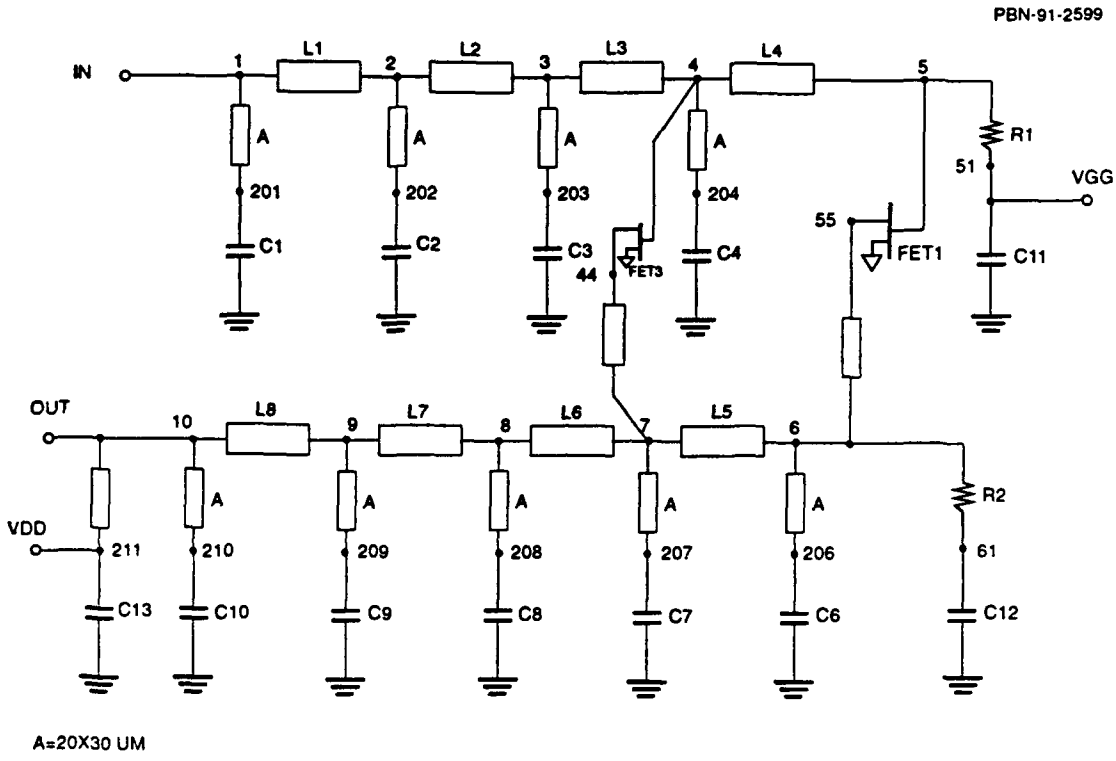


Figure 4-6. A 7.5 GHz Diplexer Small Signal Composite Response.



DIPLEXER LOW PASS SECTION - 9 GHZ

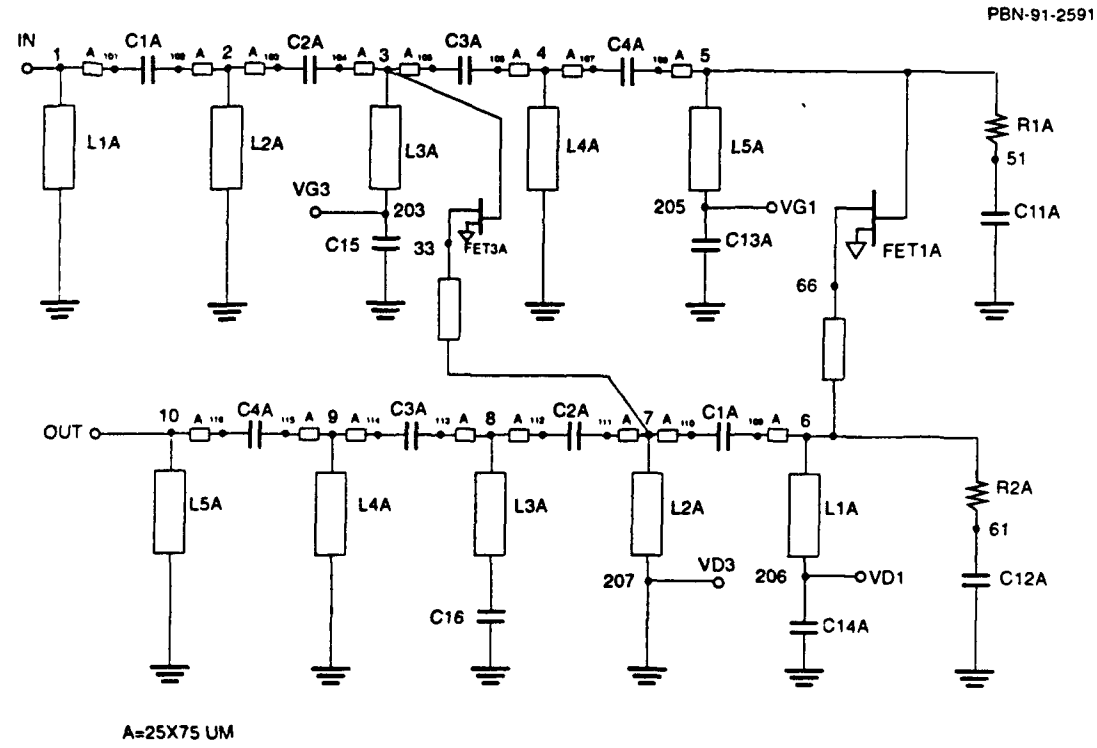


Figure 4-7. Schematic for the 9 GHz Diplexer.

PBN-91-2614

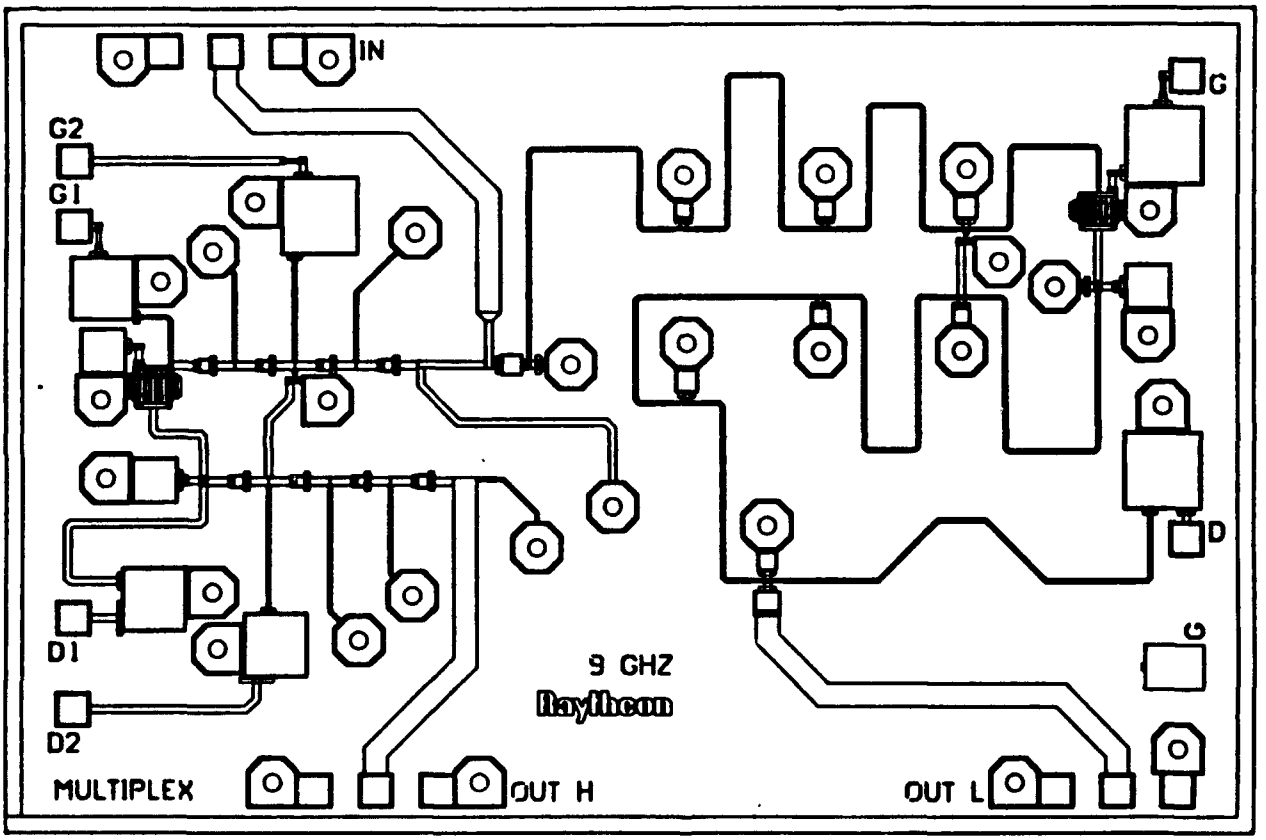


Figure 4-8. Circuit Layout for a 9 GHz Diplexer.

PBN-91-2613

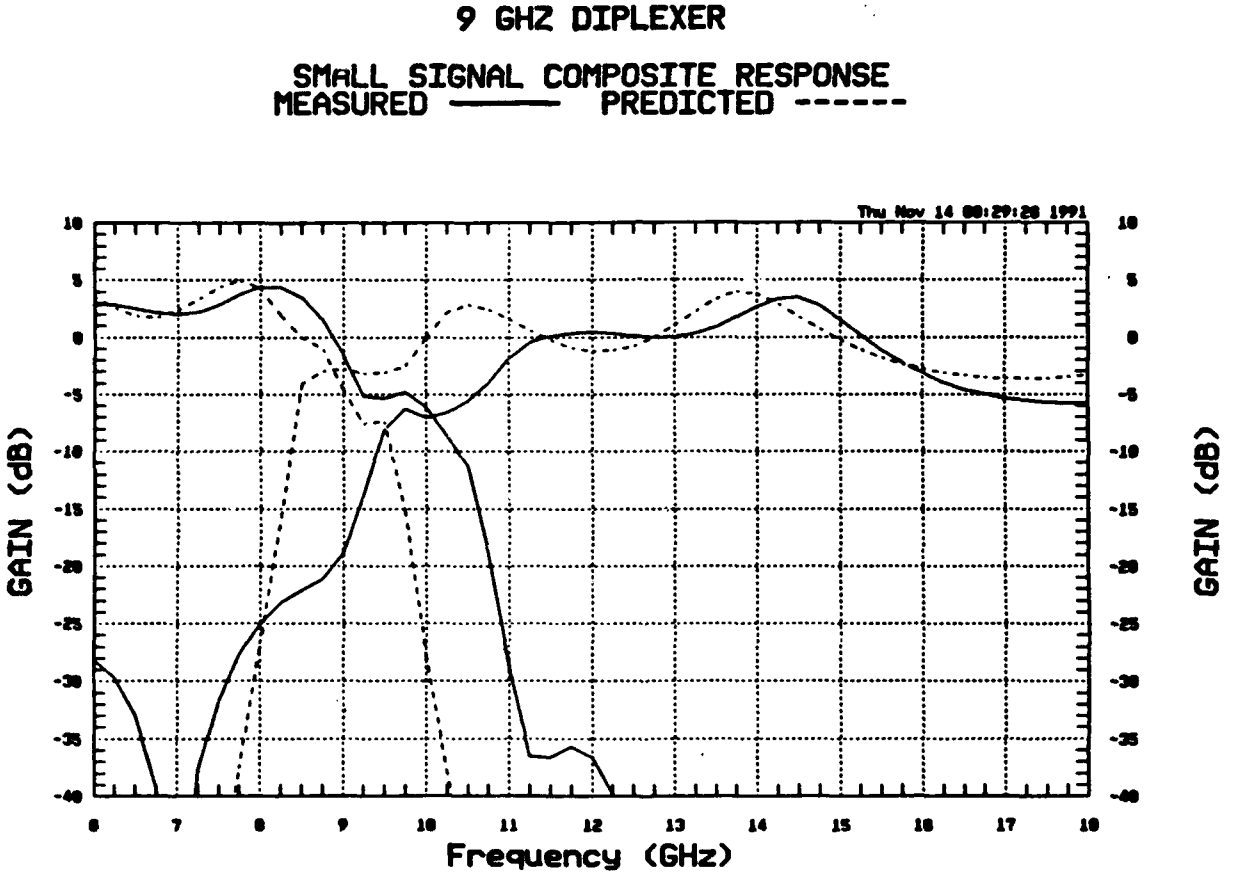
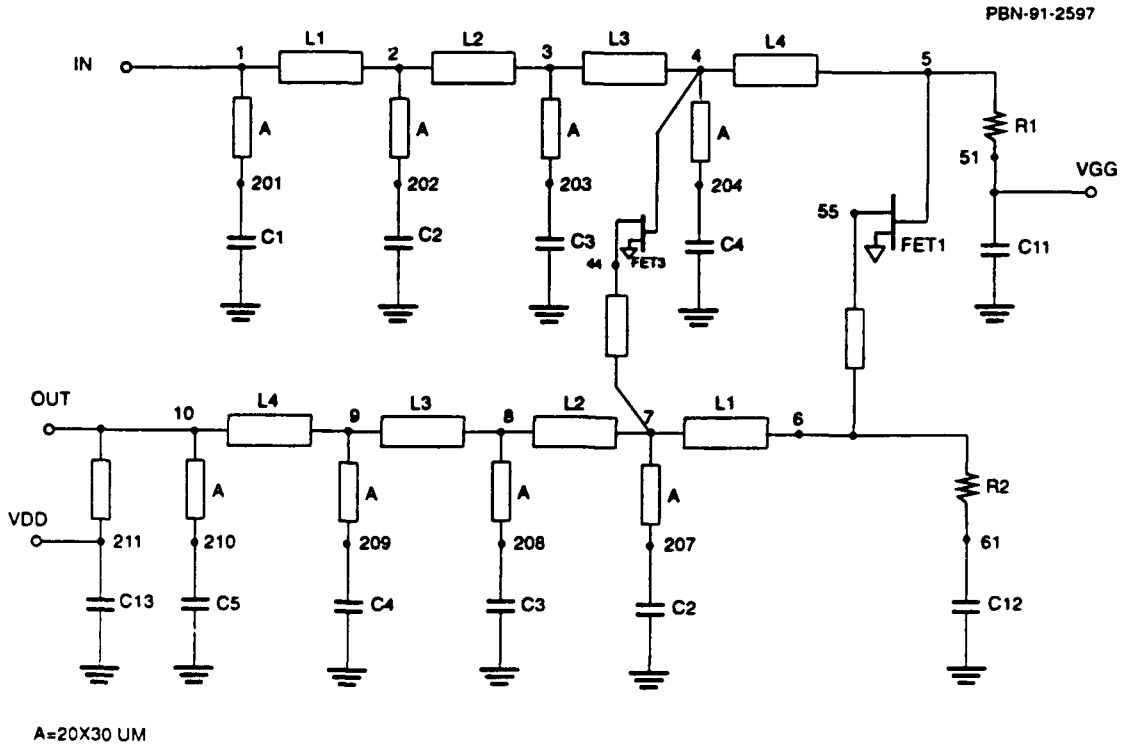


Figure 4-9. A 9 GHz Diplexer Small Signal Composite Response.



DIPLEXER LOW PASS SECTION - 10.5 GHZ

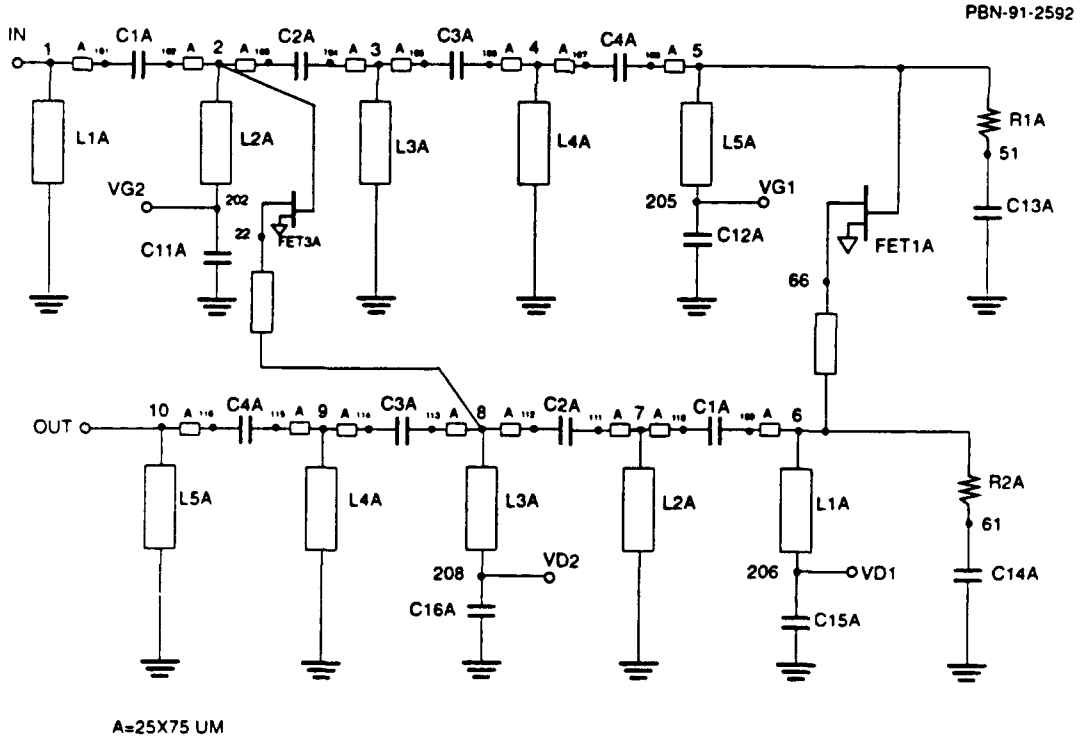


Figure 4-10. Schematic for the 10.5 GHz Diplexer.

PBN-91-2615

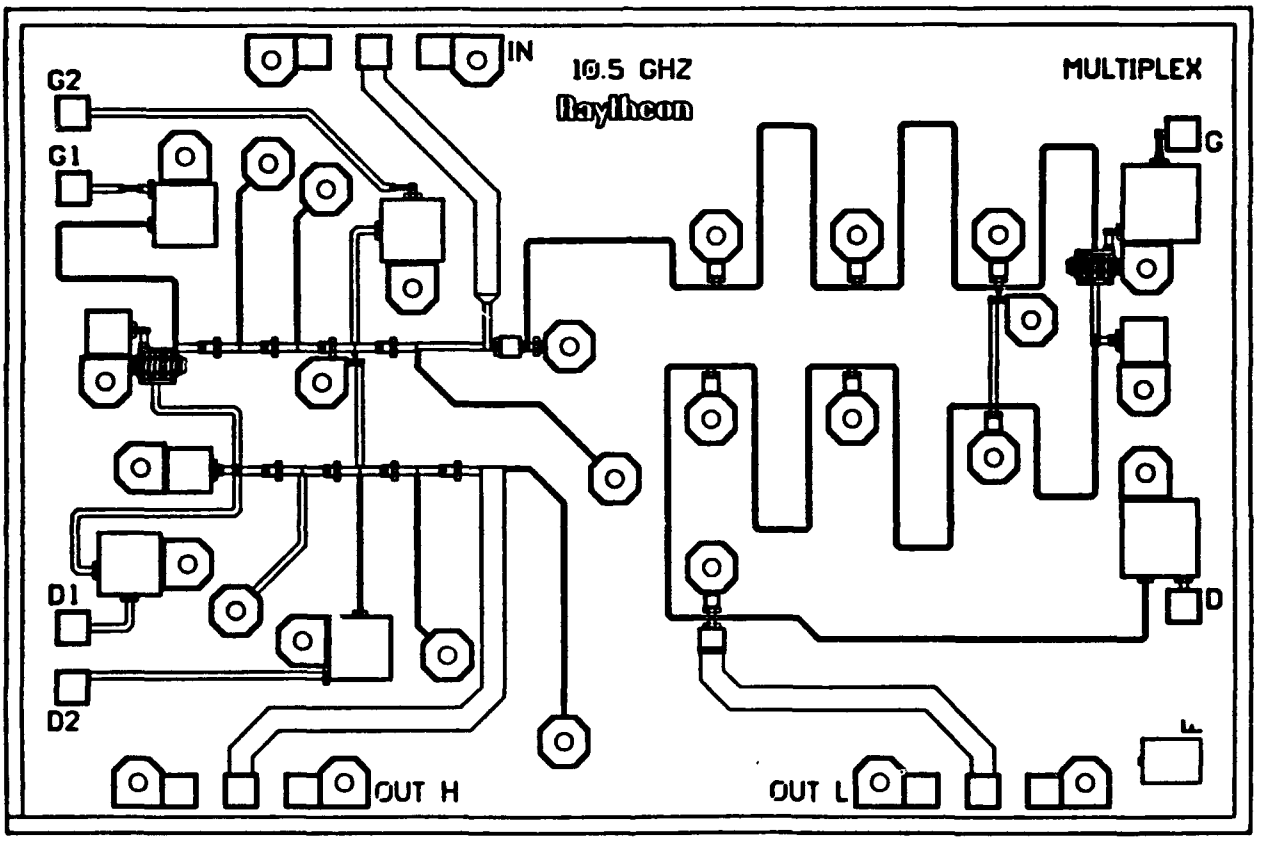


Figure 4-11. Circuit Layout for the 10.5 GHz Diplexer.

PBN-91-2644

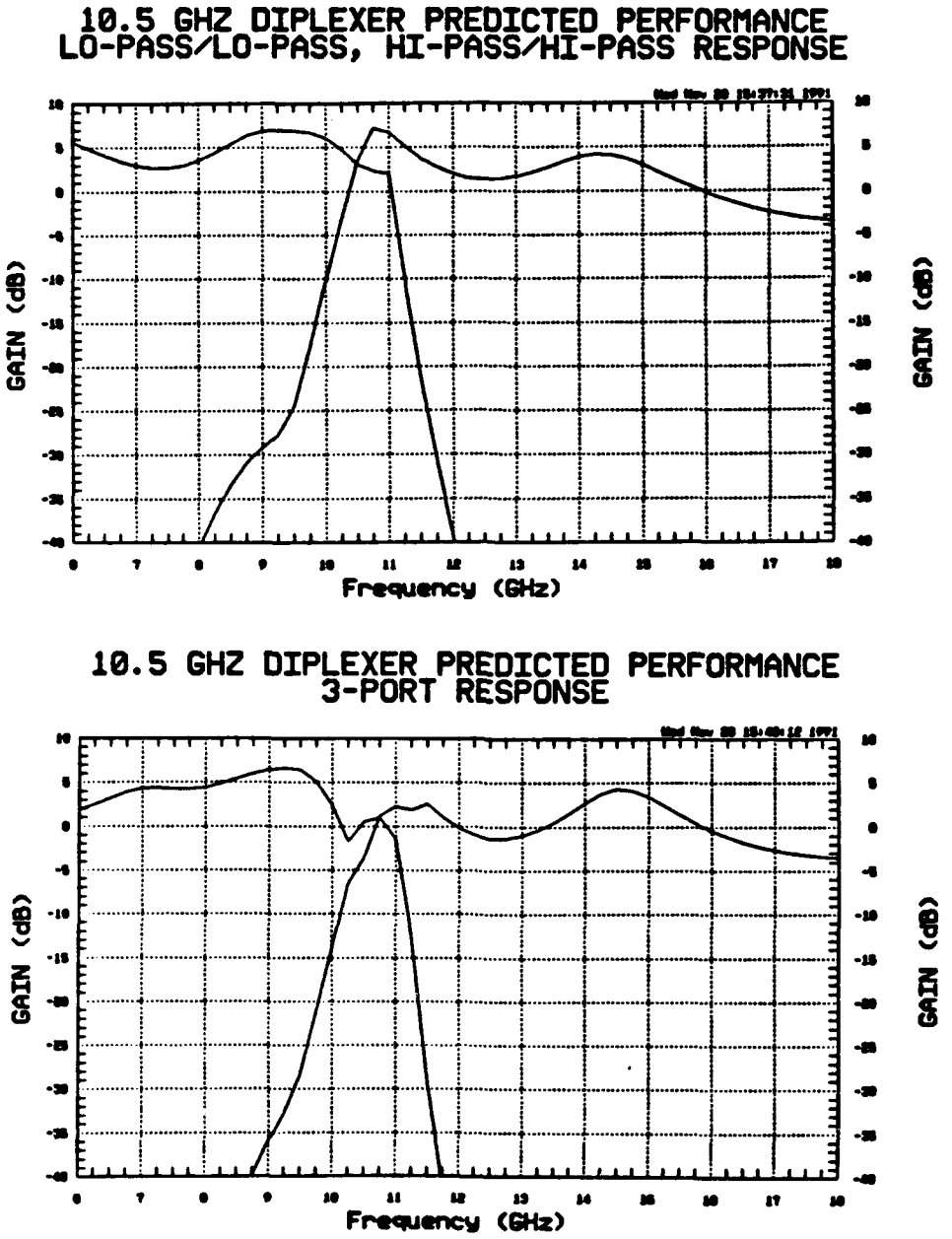


Figure 4-12. The 10.5 GHz Diplexer Predicted Performance for (a) Low Pass Low Pass/High Pass High Pass Response and (b) 3-port Response.

PBN-91-2612

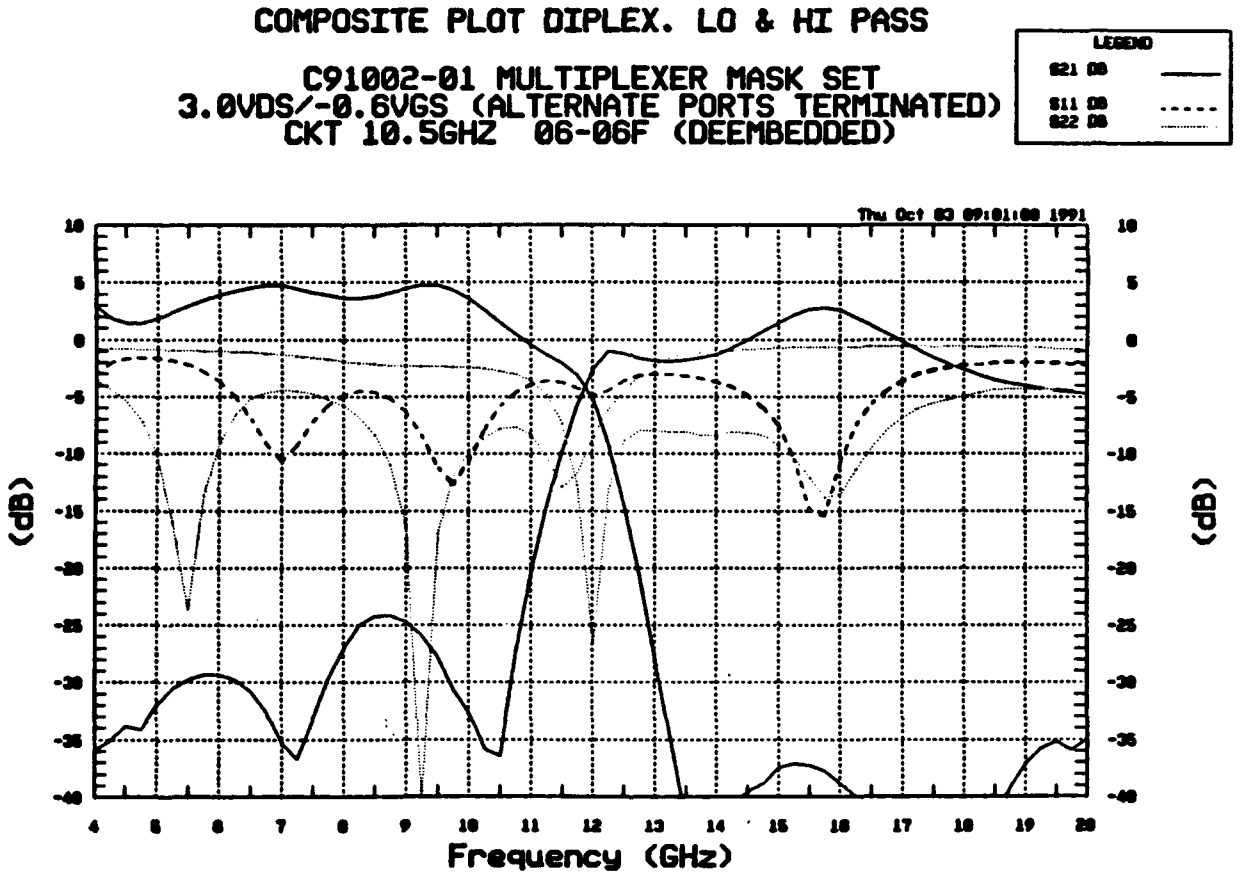


Figure 4-13. A 10.5 GHz Diplexer Small Signal Composite Response, Including S11 and S22.

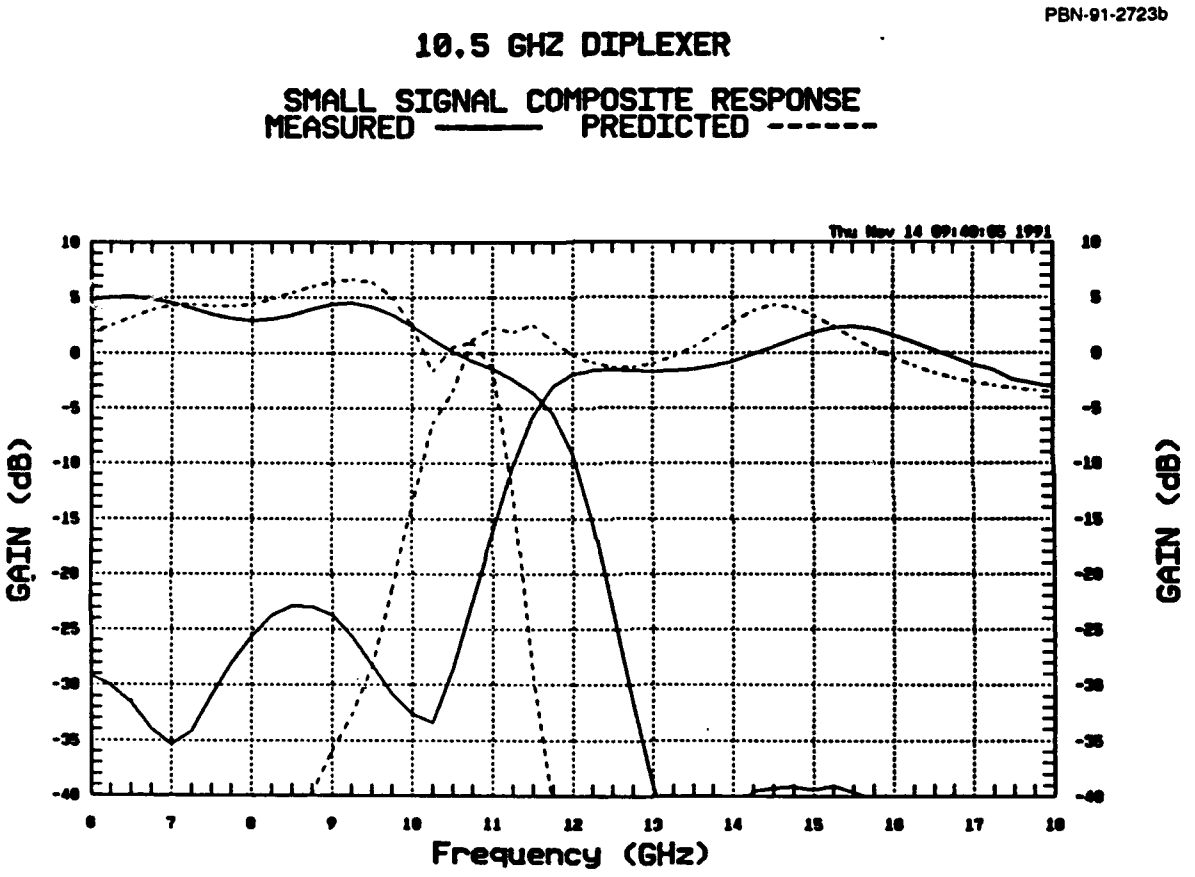
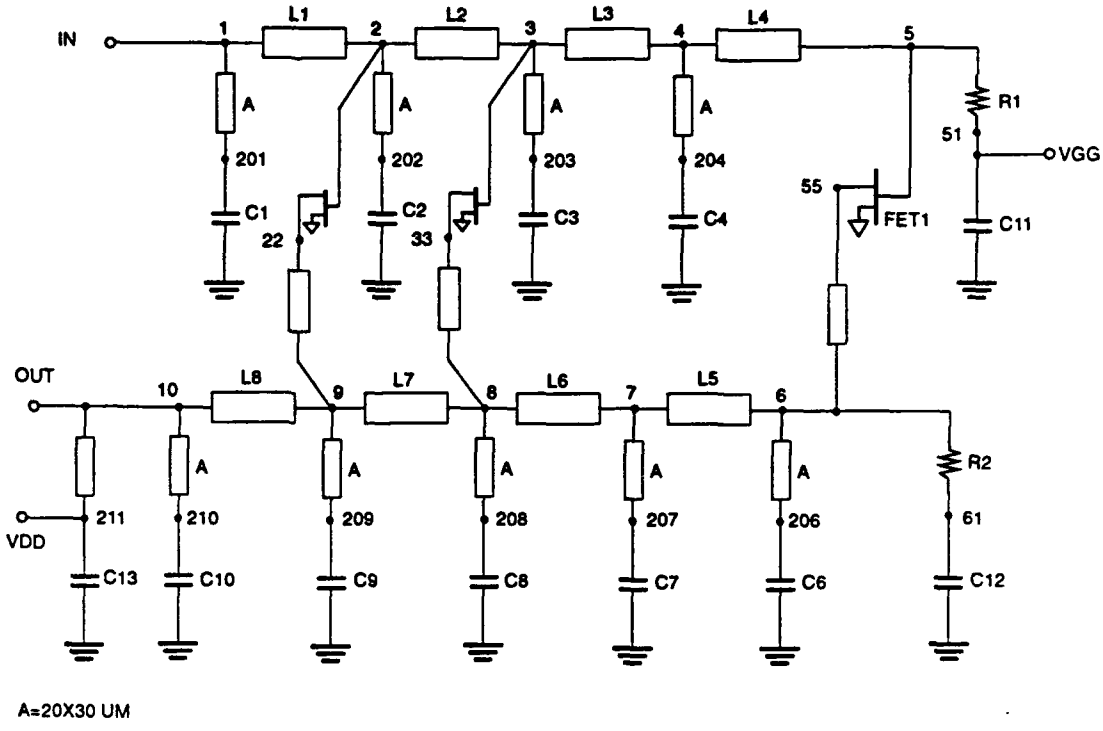


Figure 4-14. A 10.5 GHz Diplexer Small Signal Composite Response.

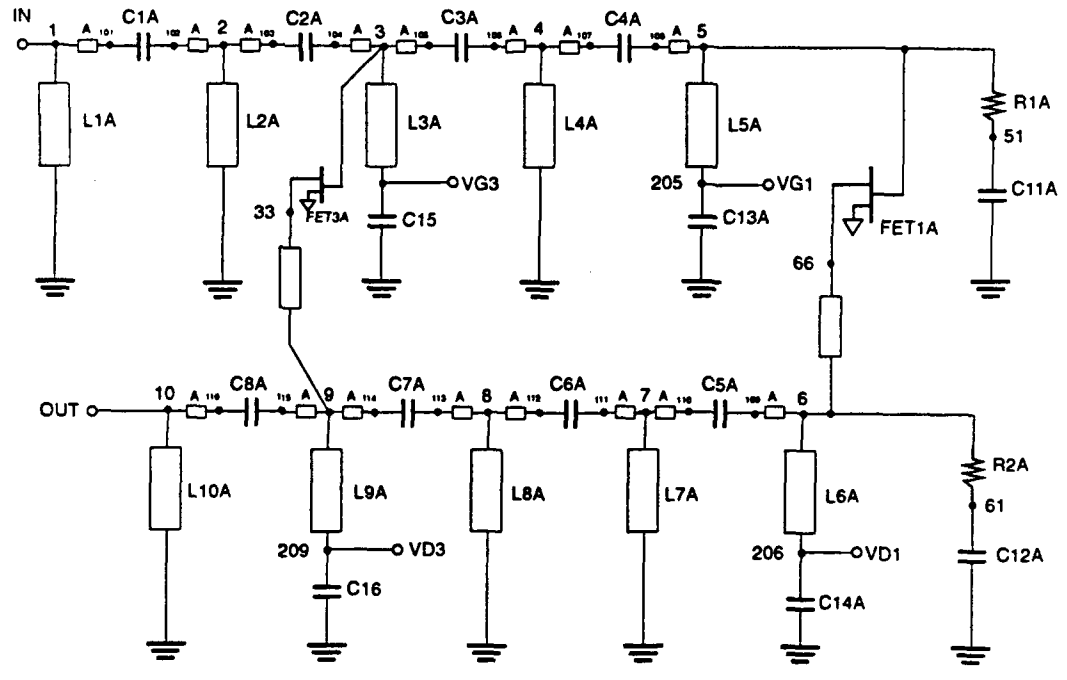
PBN-91-2600



A=20X30 UM

DIPLEXER LOW PASS SECTION - 12 GHZ

PBN-91-2593



A=25X75 UM

Figure 4-15. Schematic for the 12 GHz Diplexer.

PBN-91-2609

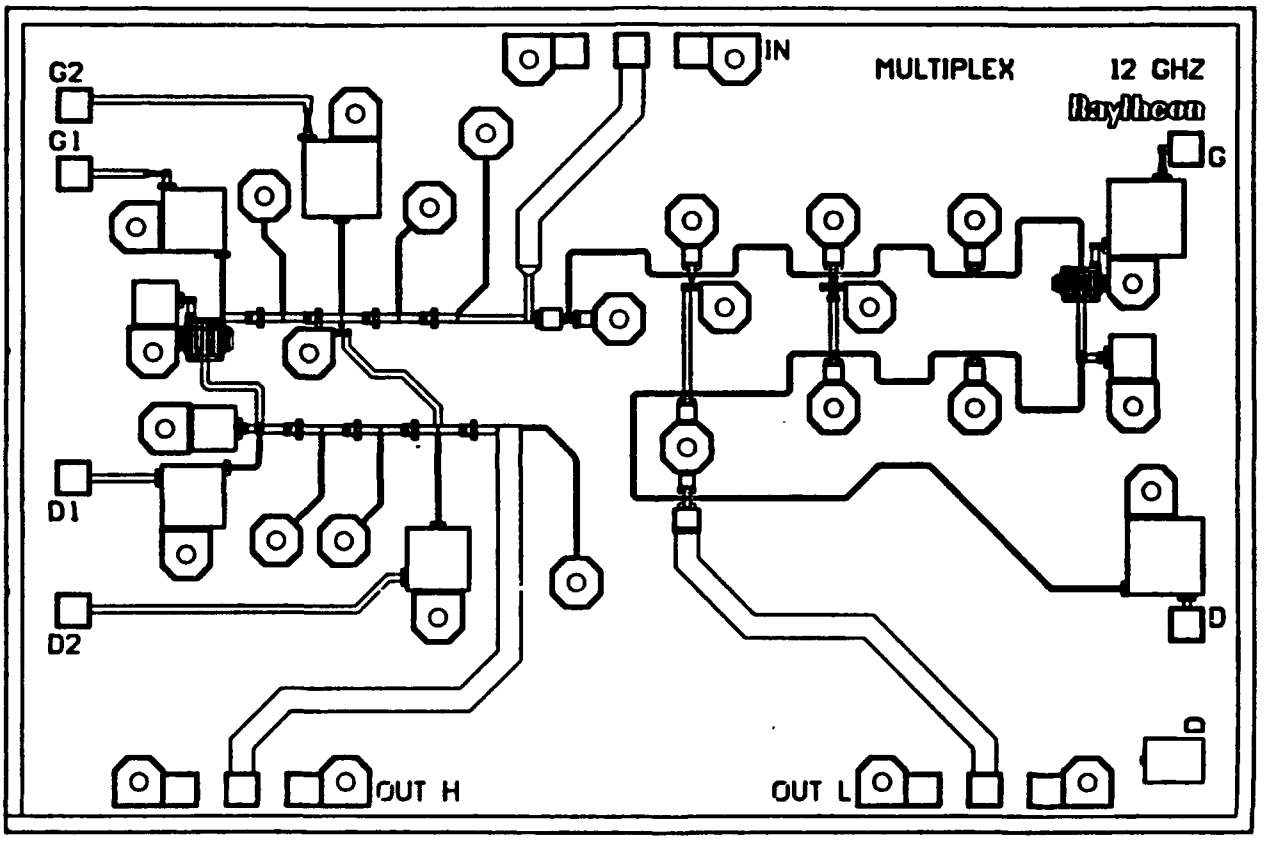


Figure 4-16. Circuit Layout for the 12 GHz Diplexer.

PBN-91-2610

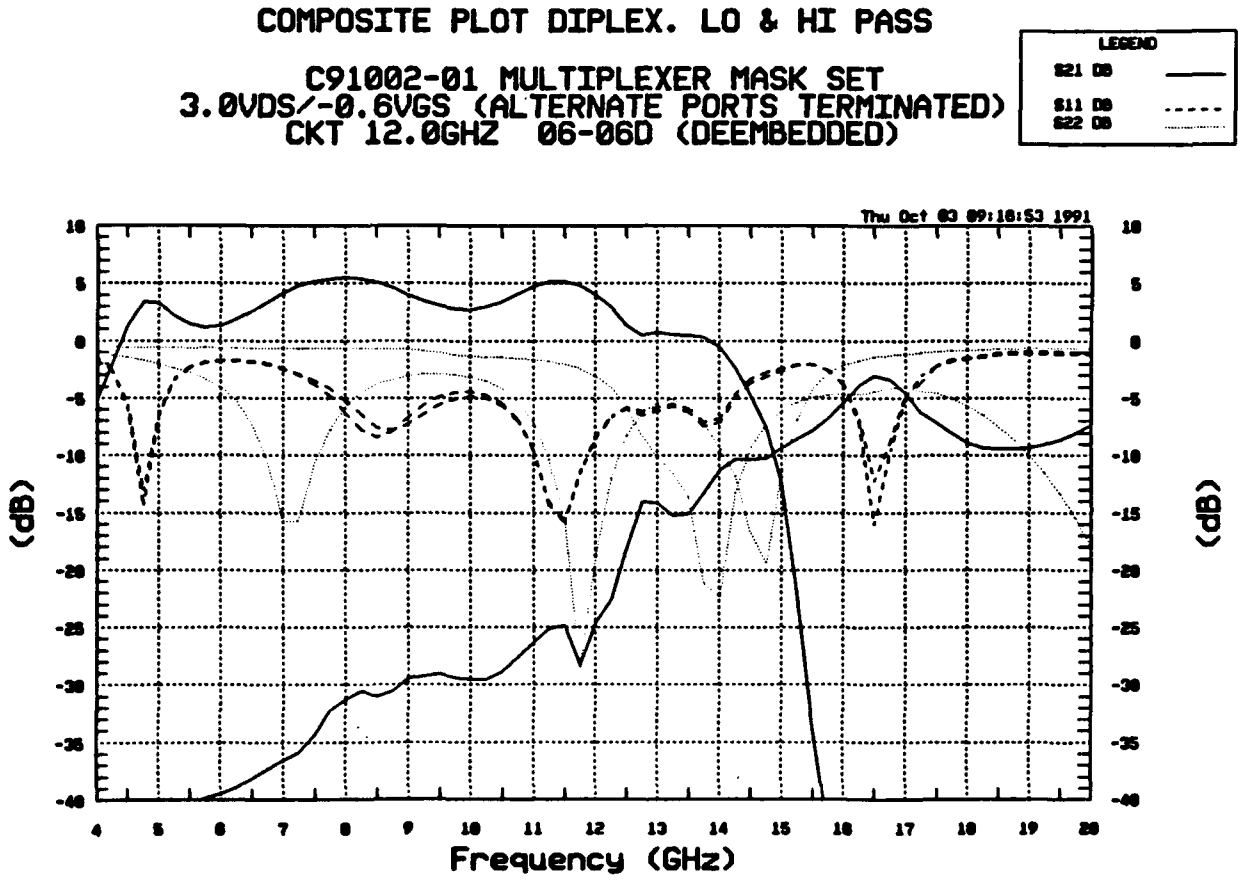


Figure 4-17. A 12 GHz Diplexer Small Signal Composite Response, Including S11 and S22.

PBN-91-2611

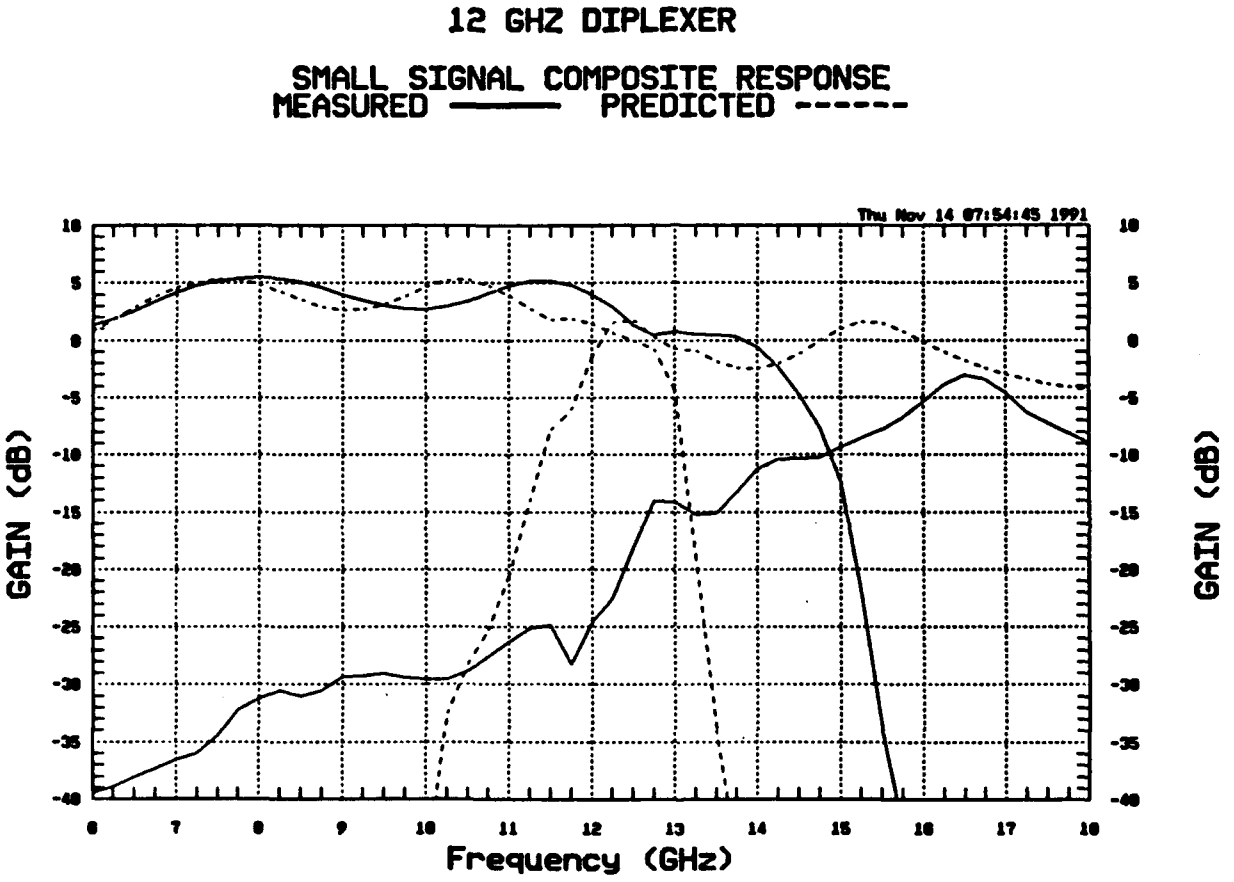
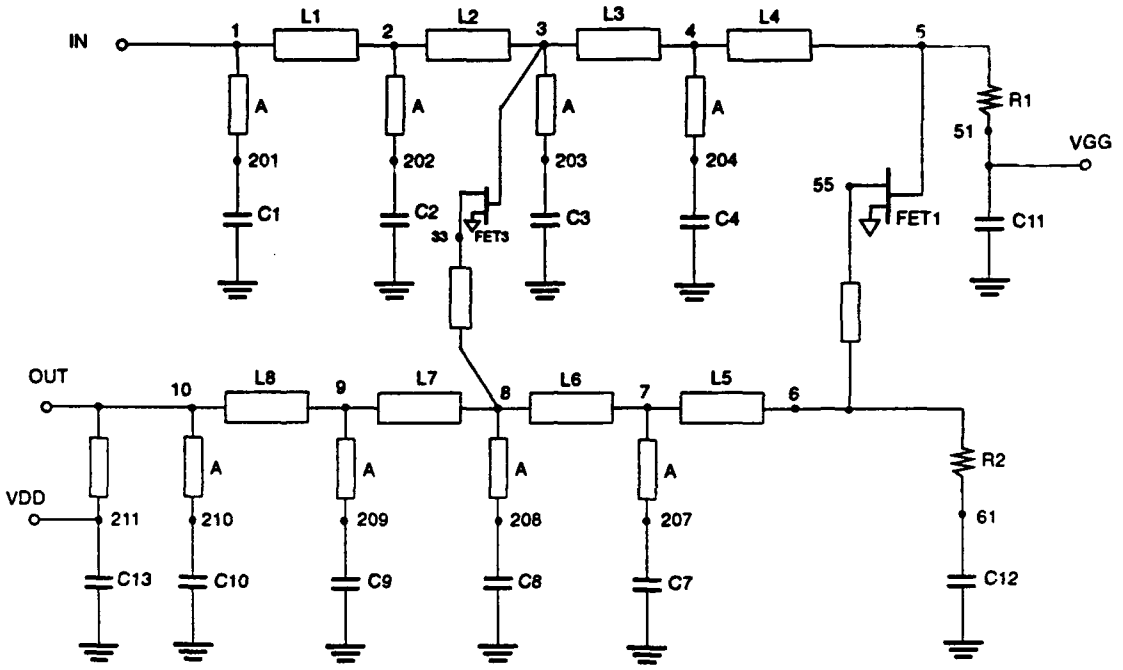


Figure 4-18. A 12 GHz Diplexer Small Signal Composite Response.

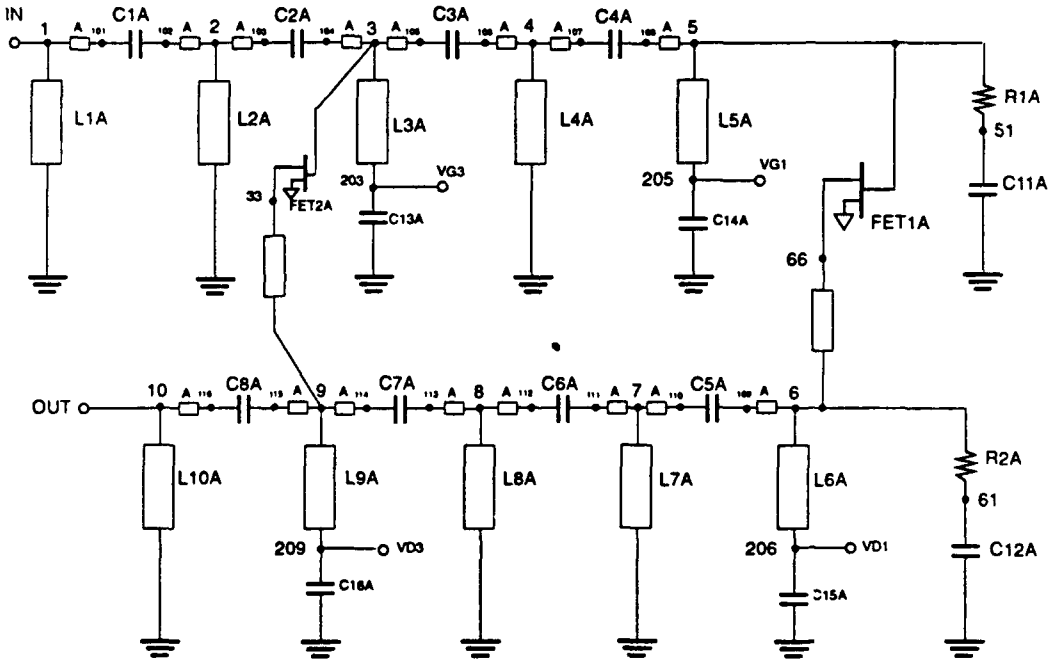
PBN-91-2601



A=20X30 UM

DIPLEXER LOW PASS SECTION - 13.5 GHZ

PBN-91-2594



A=25X75 UM

Figure 4-19. Schematic for the 13.5 GHz Diplexer.

PBN-91-2607

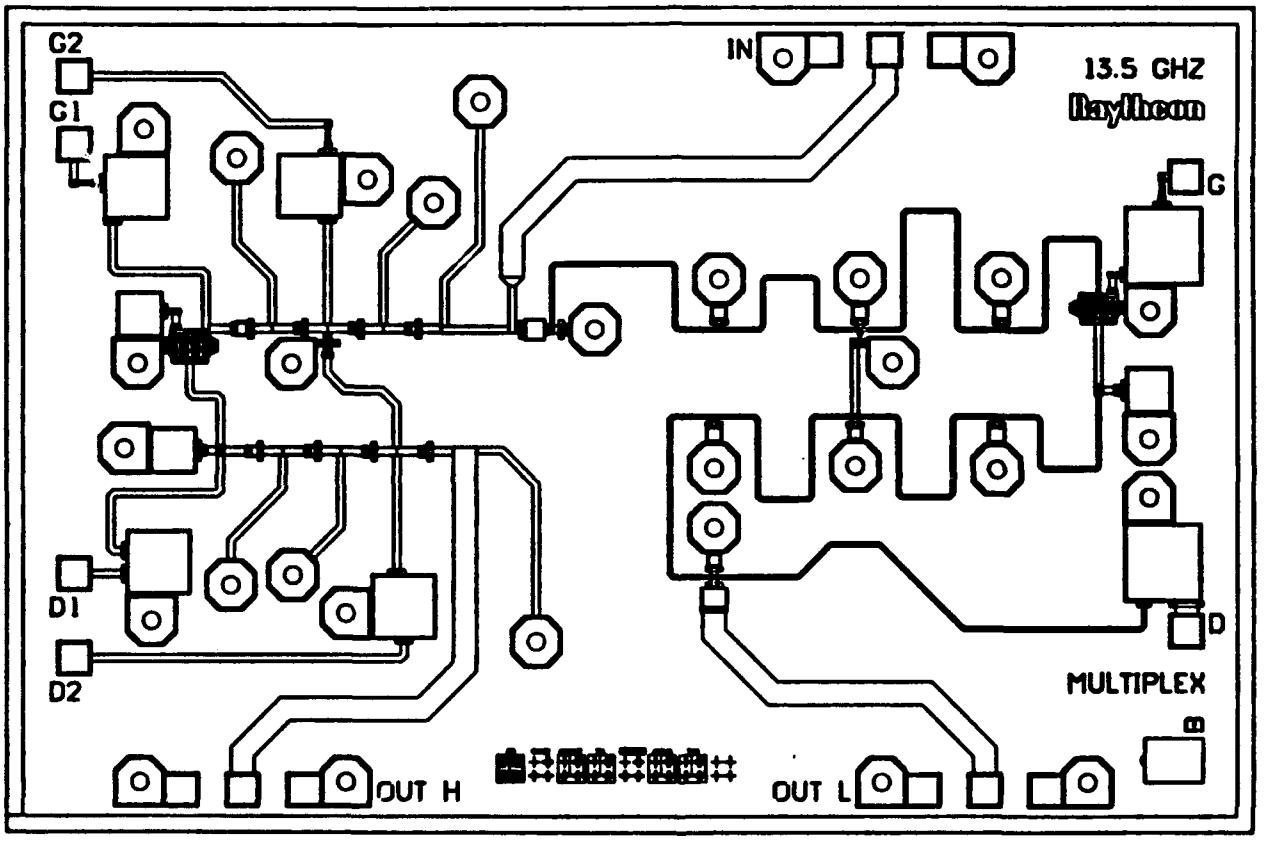


Figure 4-20. Circuit Layout for the 13.5 GHz Diplexer.

PBN-91-2608

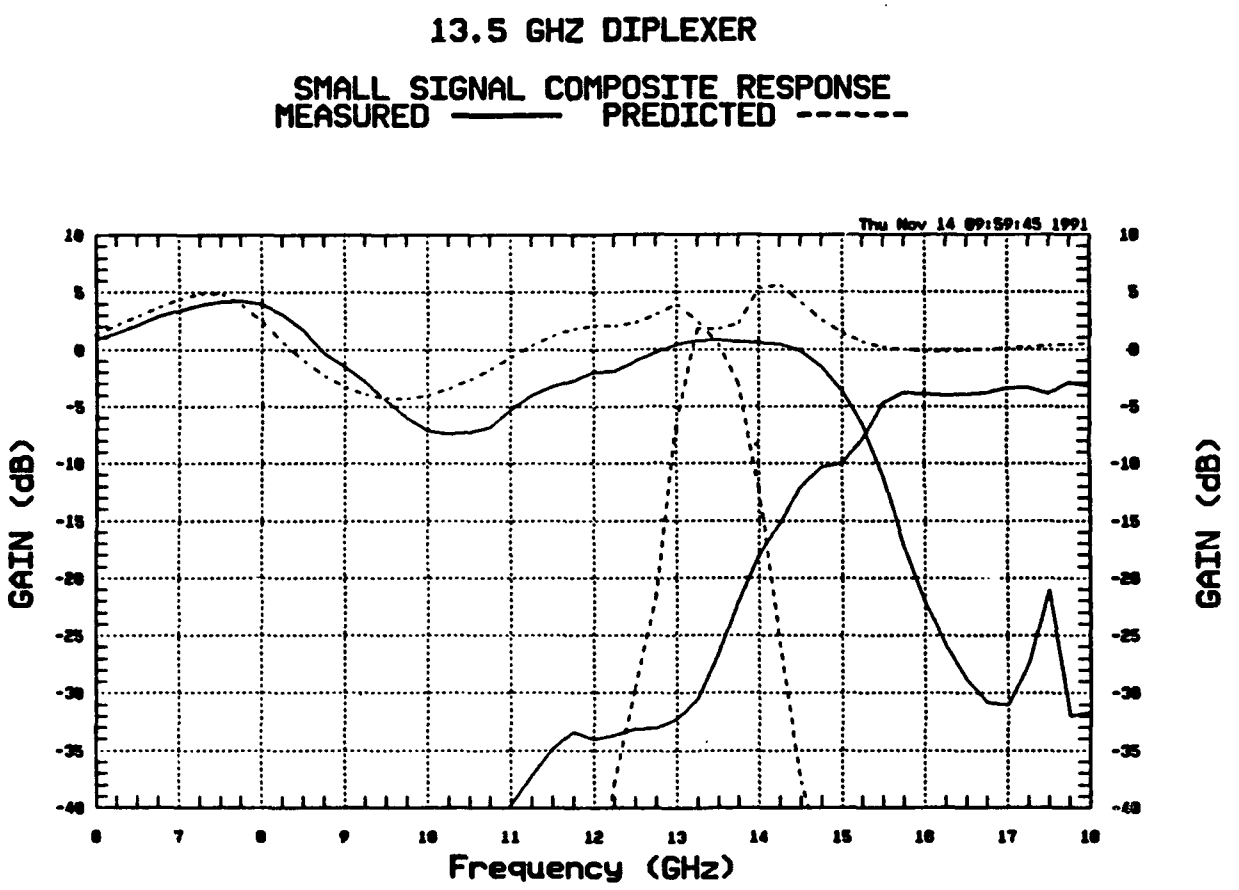
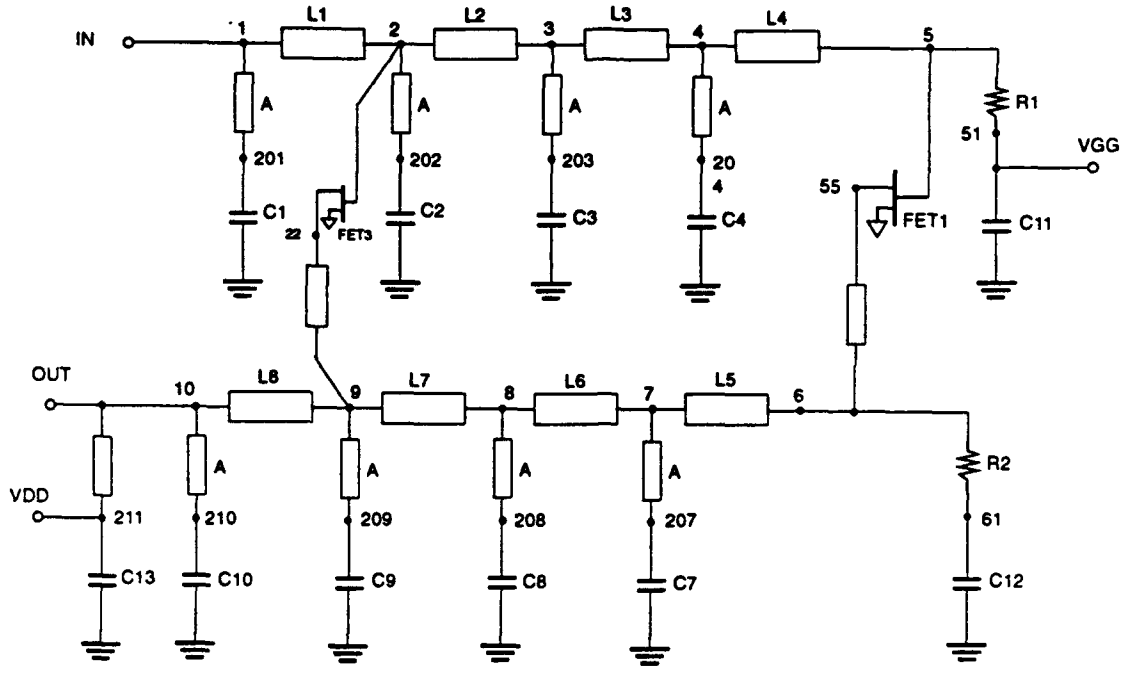


Figure 4-21. A 13.5 GHz Diplexer Small Signal Composite Response.

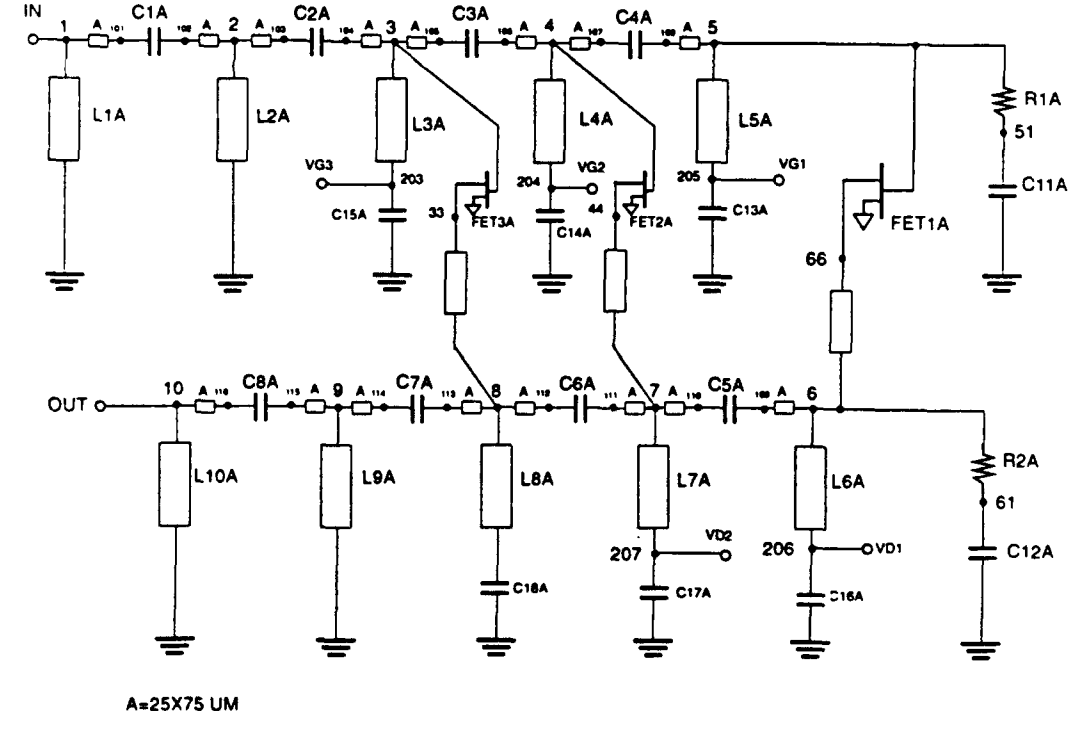
PBN-91-2602



A=20X30 UM

DIPLEXER LOW PASS SECTION - 15 GHZ

PBN-91-2595



A=25X75 UM

Figure 4-22. Schematic for the 15 GHz Diplexer.

PBN-91-2723c

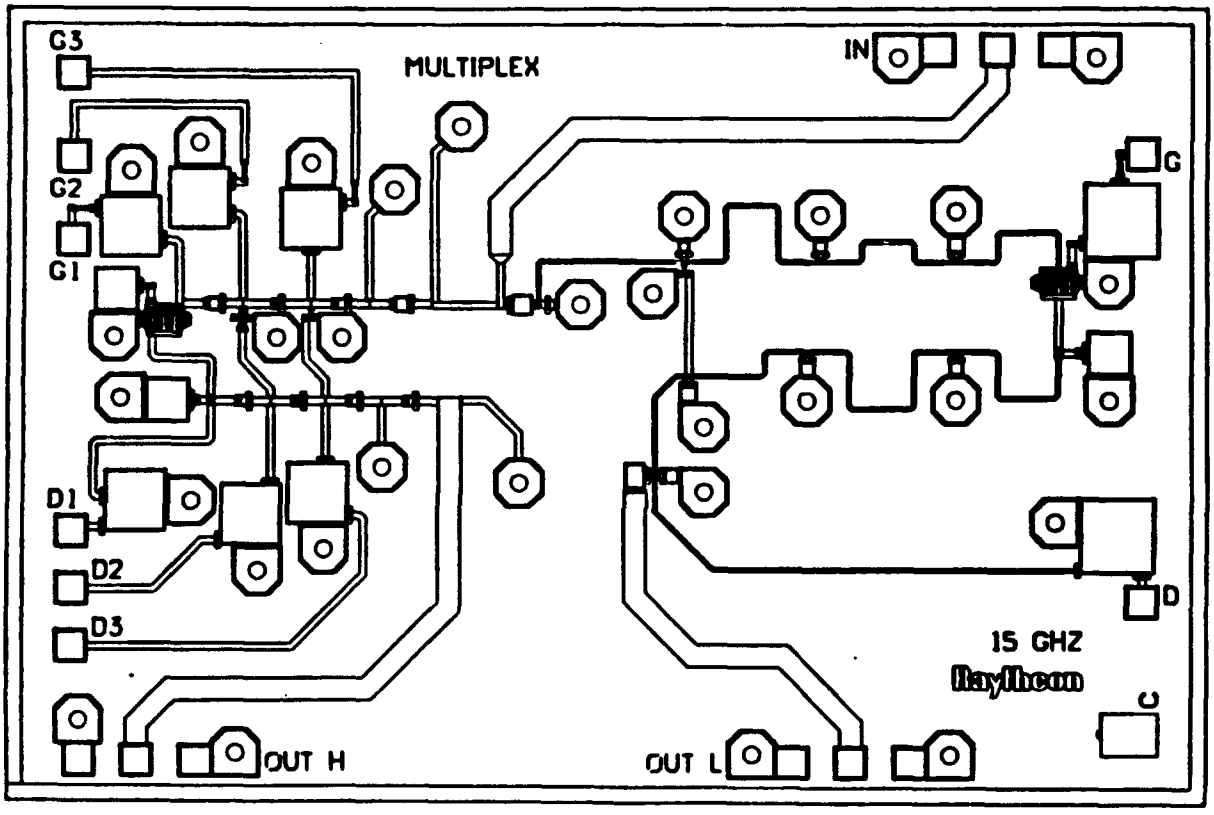


Figure 4-23. Circuit Layout for the 15 GHz Diplexer.

PBN-91-2606

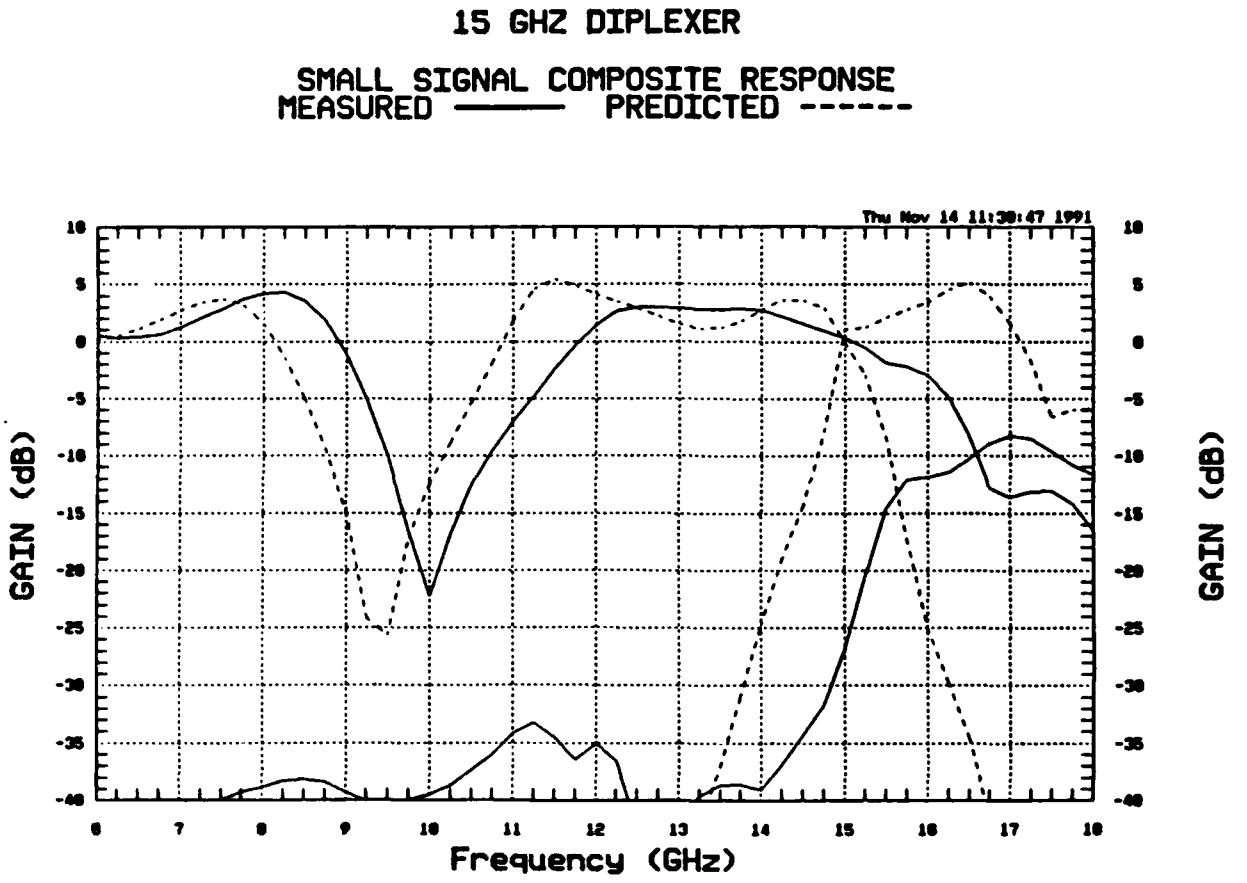
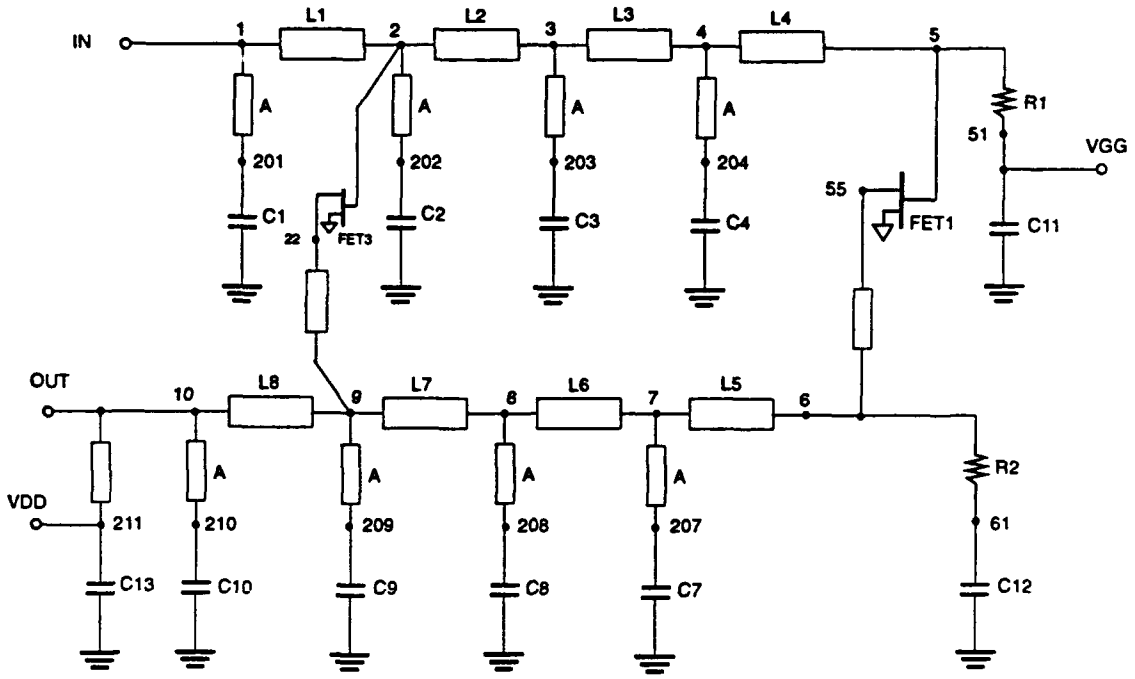


Figure 4-24. A 15 GHz Diplexer Small Signal Composite Response.

PBN-91-2603



DIPLEXER LOW PASS SECTION - 16.5 GHZ

PBN-91-2596

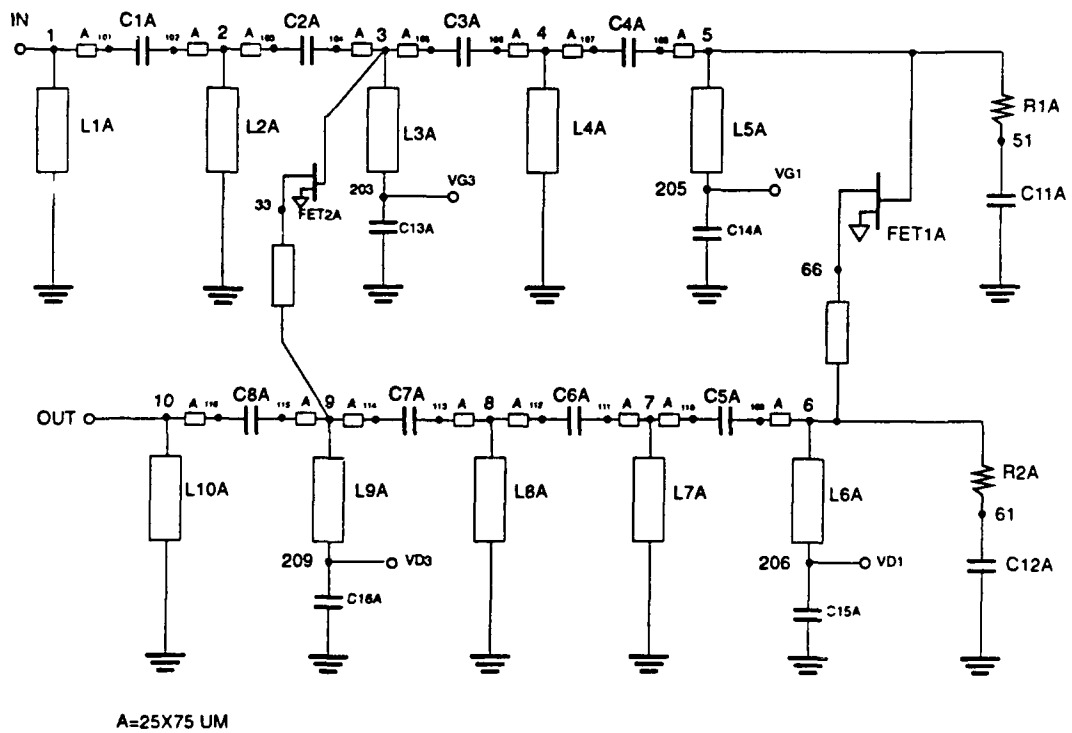


Figure 4-25. Schematic for the 16.5 GHz Diplexer.

PBN-91-2723d

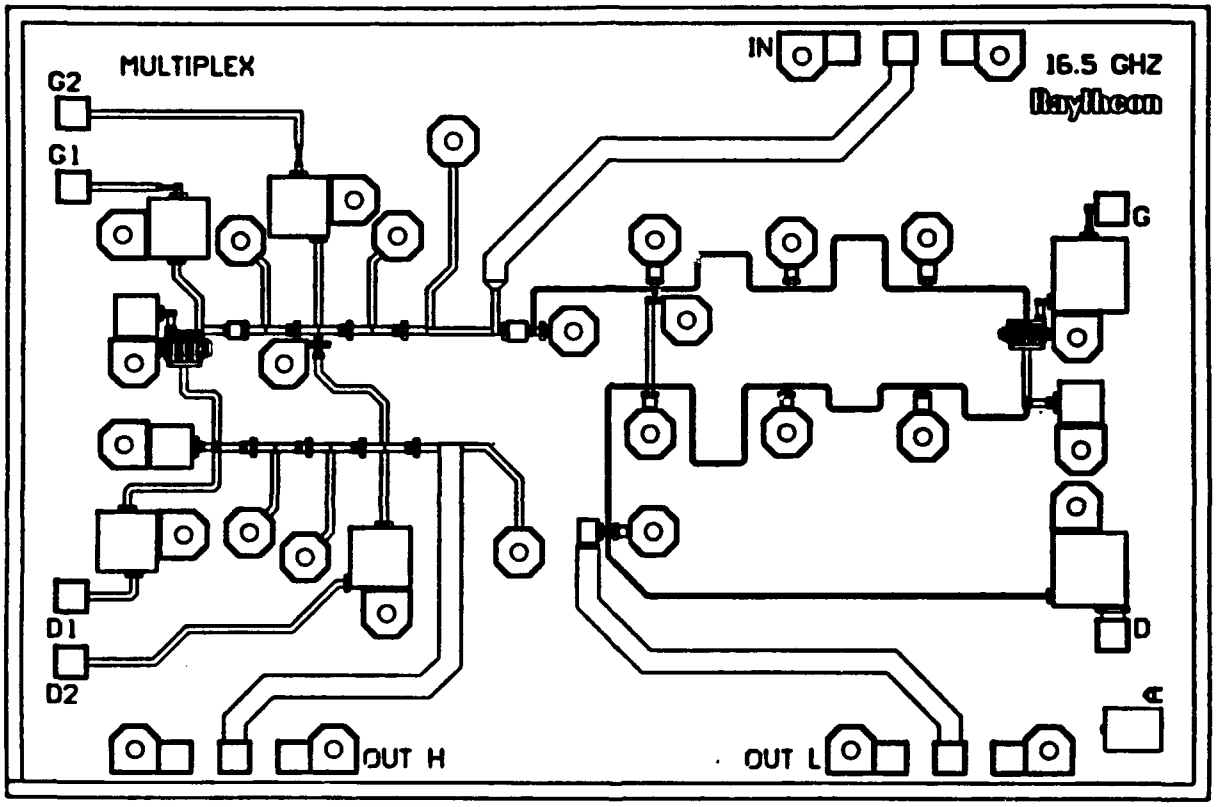


Figure 4-26. Circuit Layout for the 16.5 GHz Diplexer.

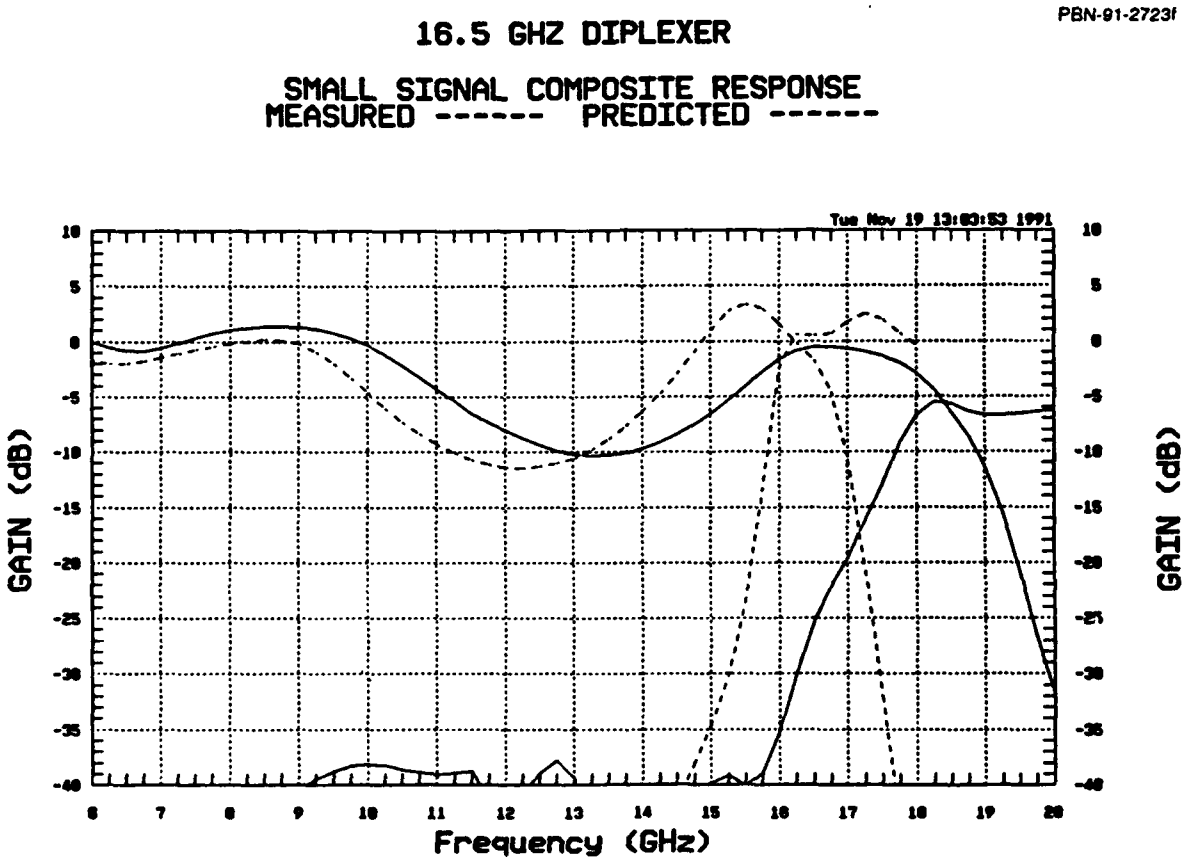


Figure 4-27. A 16.5 GHz Diplexer Small Signal Composite Response.

5.0 MULTIPLEXER CHARACTERIZATION

The multiplexer module is assembled on a single carrier using seven diplexer chips as shown in Figure 5-1. Each channel is measured by sliding the output half of the test fixture, Figure 5-2, and by pressure contact between the carrier RF line and the fixture center pin. The unused ports are left unterminated; this has a minimal effect on the channel being measured.

5.1 Multiplexer Assembly

The diplexer chips, the required dc biasing components, and the RF components were assembled on a carrier as shown in Figure 5-1. This carrier was assembled in a test fixture which connects to the multiplexer through pressure contact between the fixture block RF pin and the carrier alumina RF line. The output half of the fixture is slid to make pressure contact with various RF output ports of the multiplexer.

Figure 5-3 shows a fully assembled multiplexer module in the test fixture.

5.2 Performance

Figures 5-4 through 5-11 show the small signal performance of the multiplexer for channels 1 through 8 respectively. The multiplexer was fully turned on and biased at 3.0 V_{ds}, -0.6 V_{gs}. The total I_{ds} for module no. 1 was 680 mA and for module no. 2, 470 mA. The unused ports were not terminated during the measurement. Figure 5-12 is a composite response for multiplexer module no. 1 and Figure 5-14 is the multiplexer module no. 2 response. Both multiplexers were delivered as part of the contract requirement.

Figure 5-13 shows the measured and predicted response for multiplexer module no 1. The 12 GHz low pass filter was turned off for measurements on channels 5 through 8 to show the potential improvement when the coupling effects are reduced in one chip. This plot should be compared to Figure 5-12.

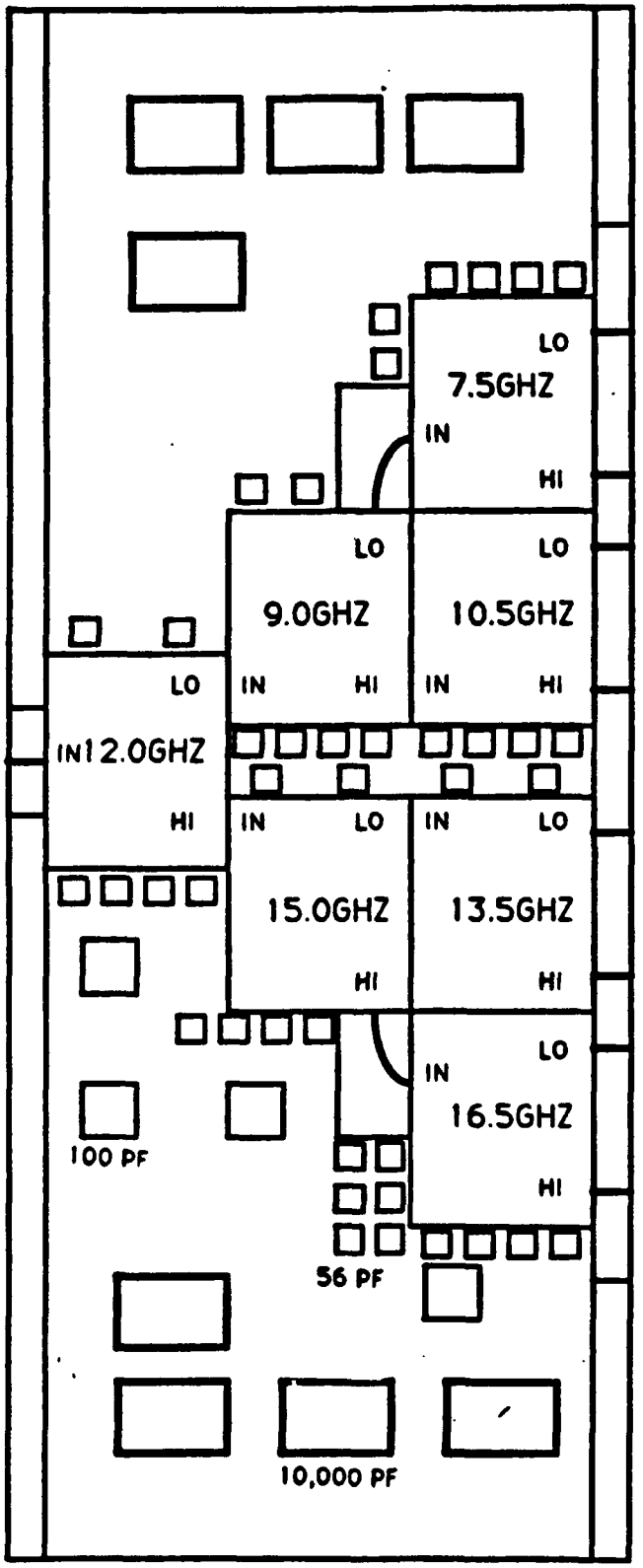


Figure 5-1. Multiplexer Carrier Assembly.

PBN-91-2635

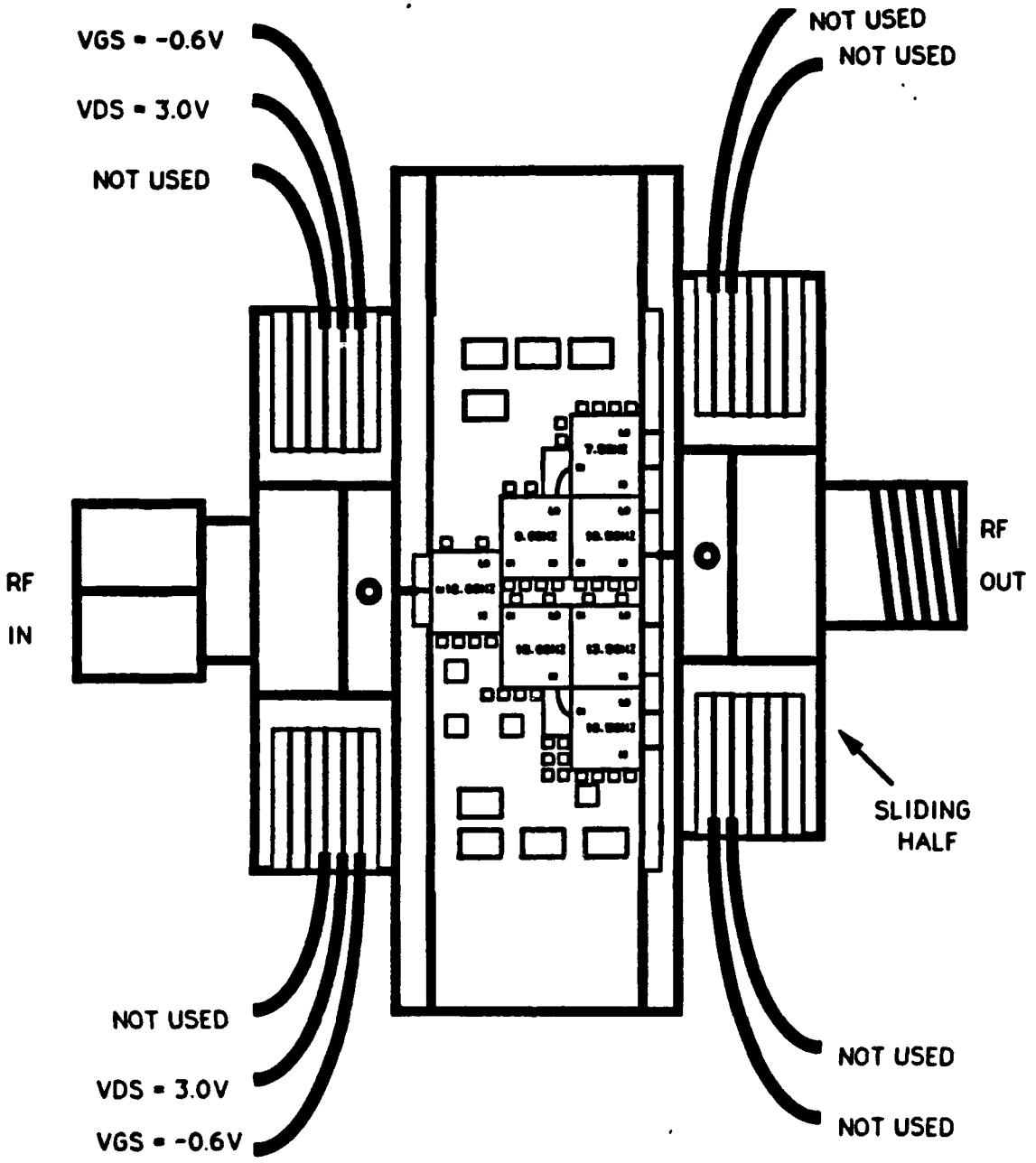


Figure 5-2. Multiplexer Module Assembly.

1CE16611

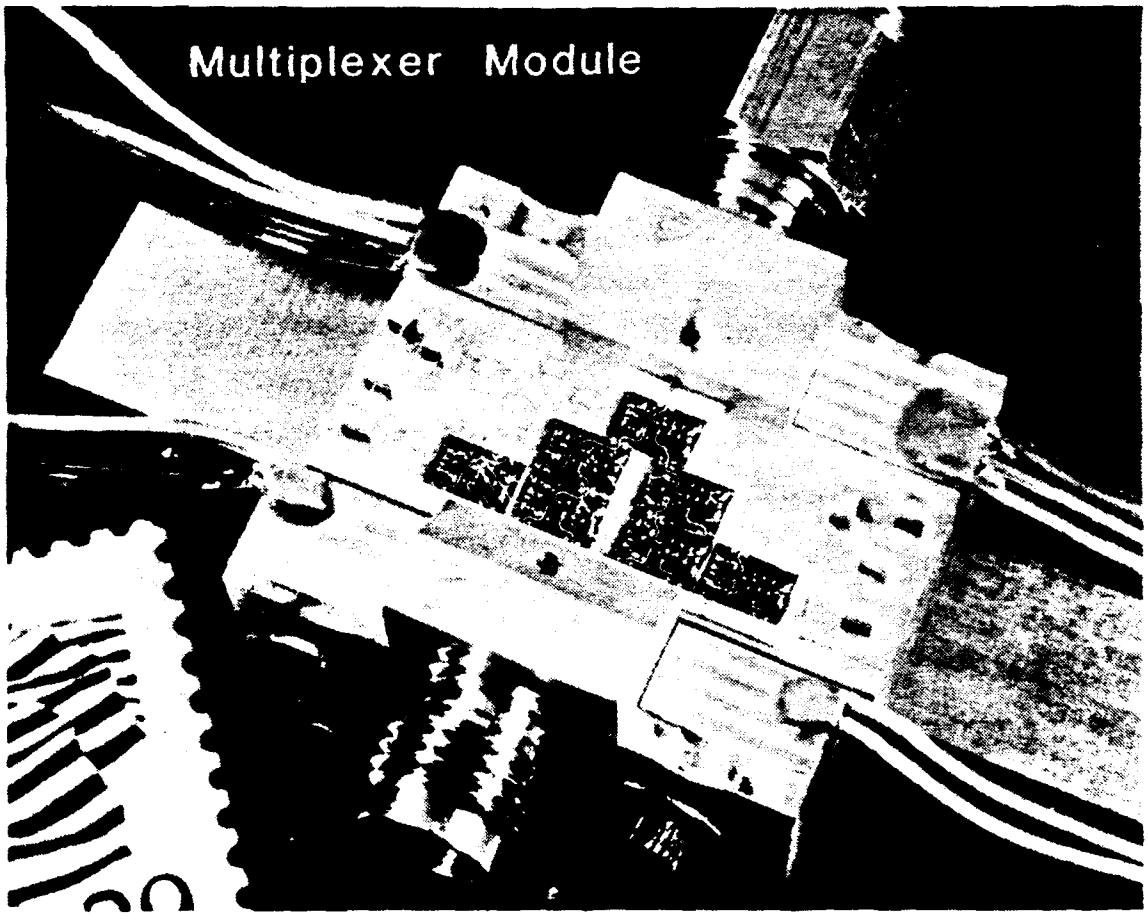


Figure 5-3. Photograph of a Multiplexer Module Assembly.

PBN-91-2623

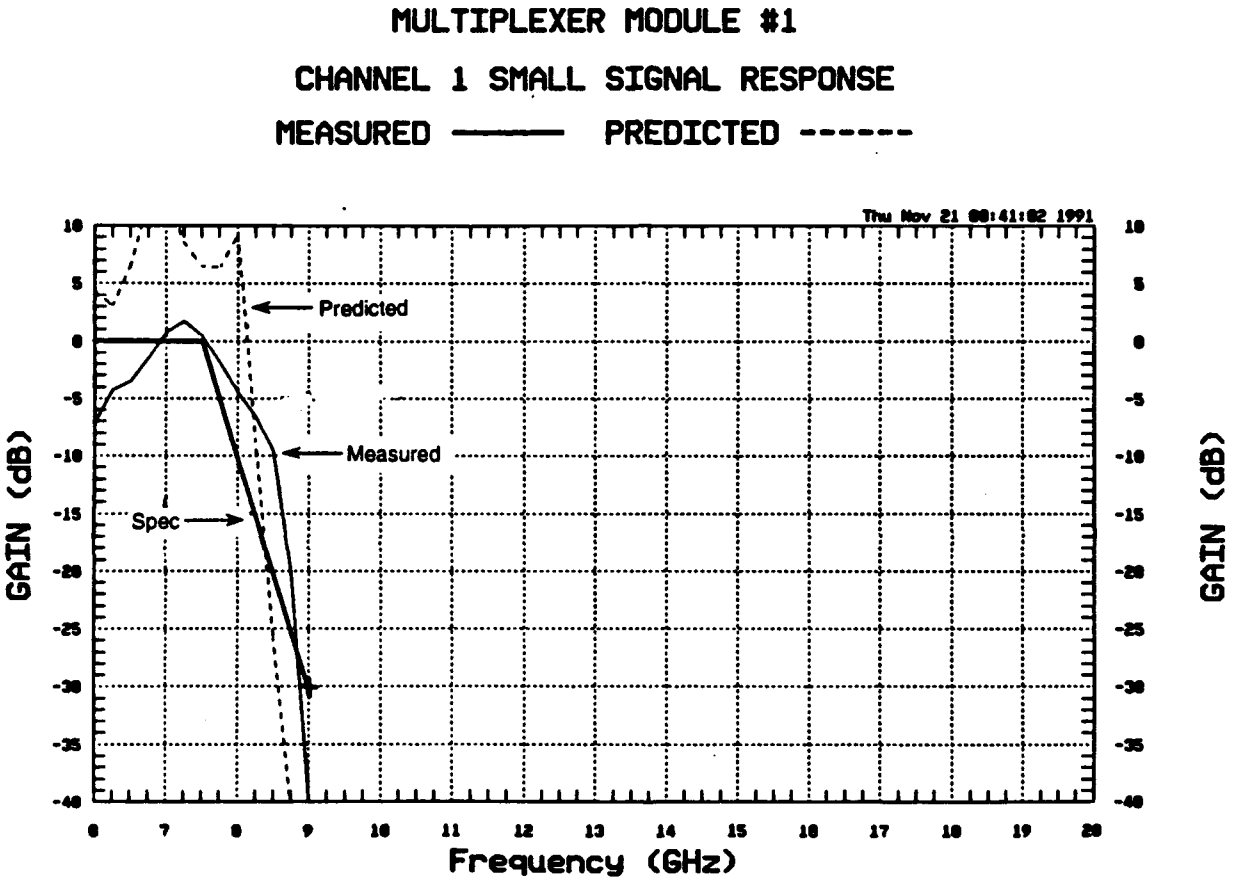


Figure 5-4. Multiplexer Performance, Channel 1 Response.

PBN-91-2624

MULTIPLEXER MODULE #1

CHANNEL 2 SMALL SIGNAL RESPONSE

MEASURED ——— PREDICTED ------

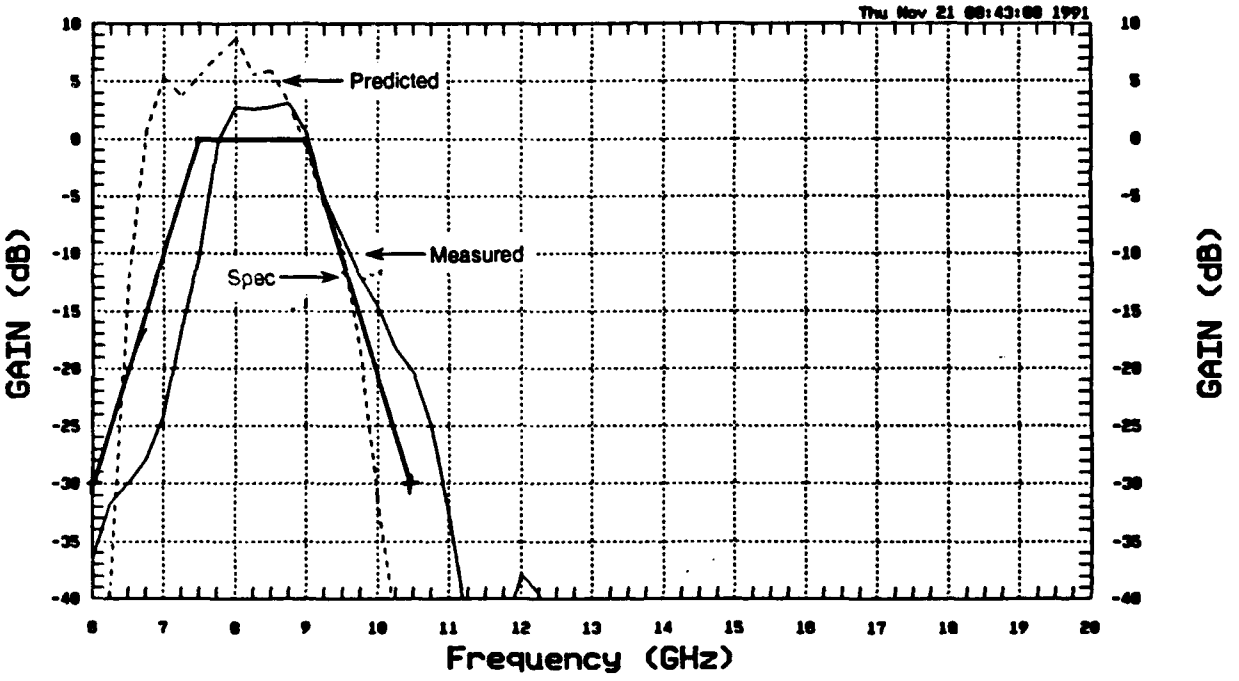


Figure 5-5. Multiplexer Performance, Channel 2 Response.

PBN-91-2625

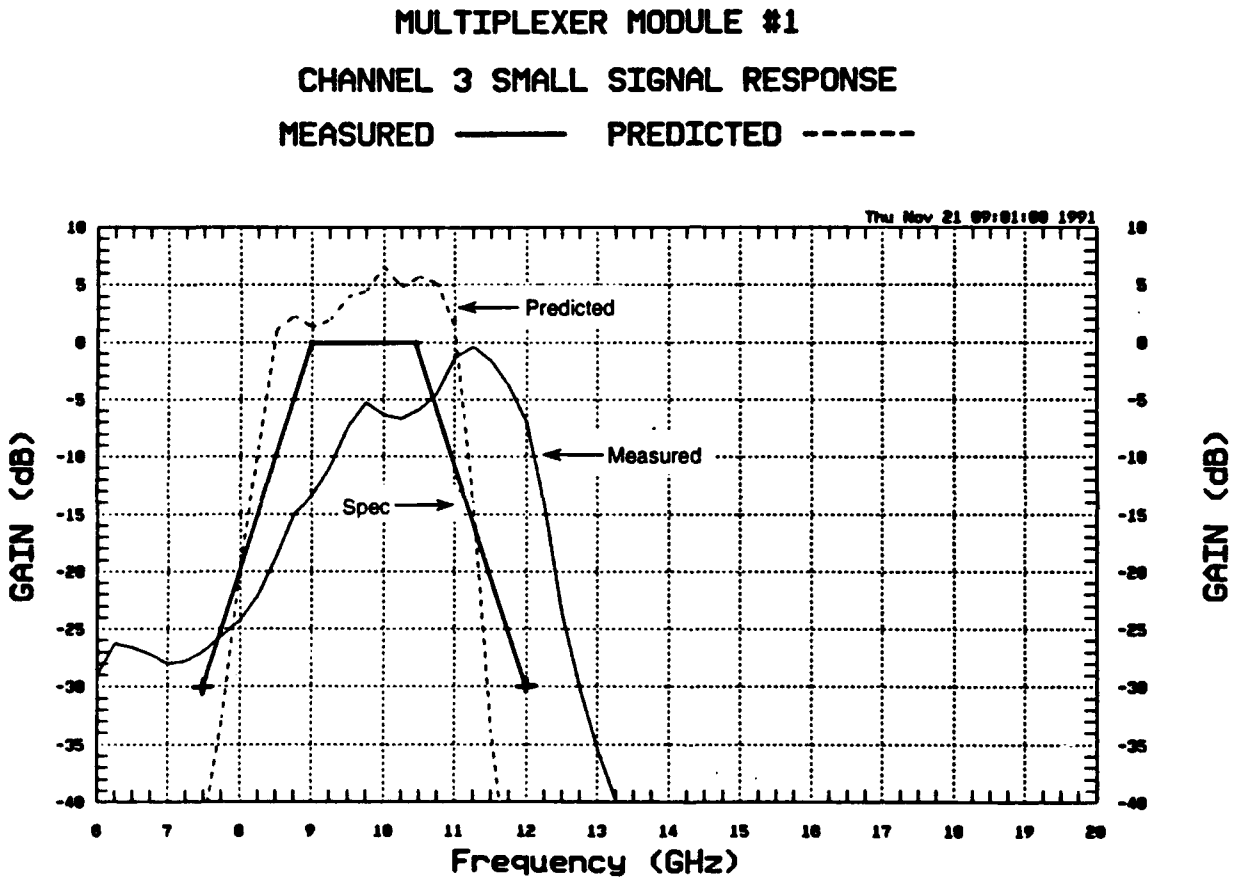


Figure 5-6. Multiplexer Performance, Channel 3 Response.

PBN-91-2626

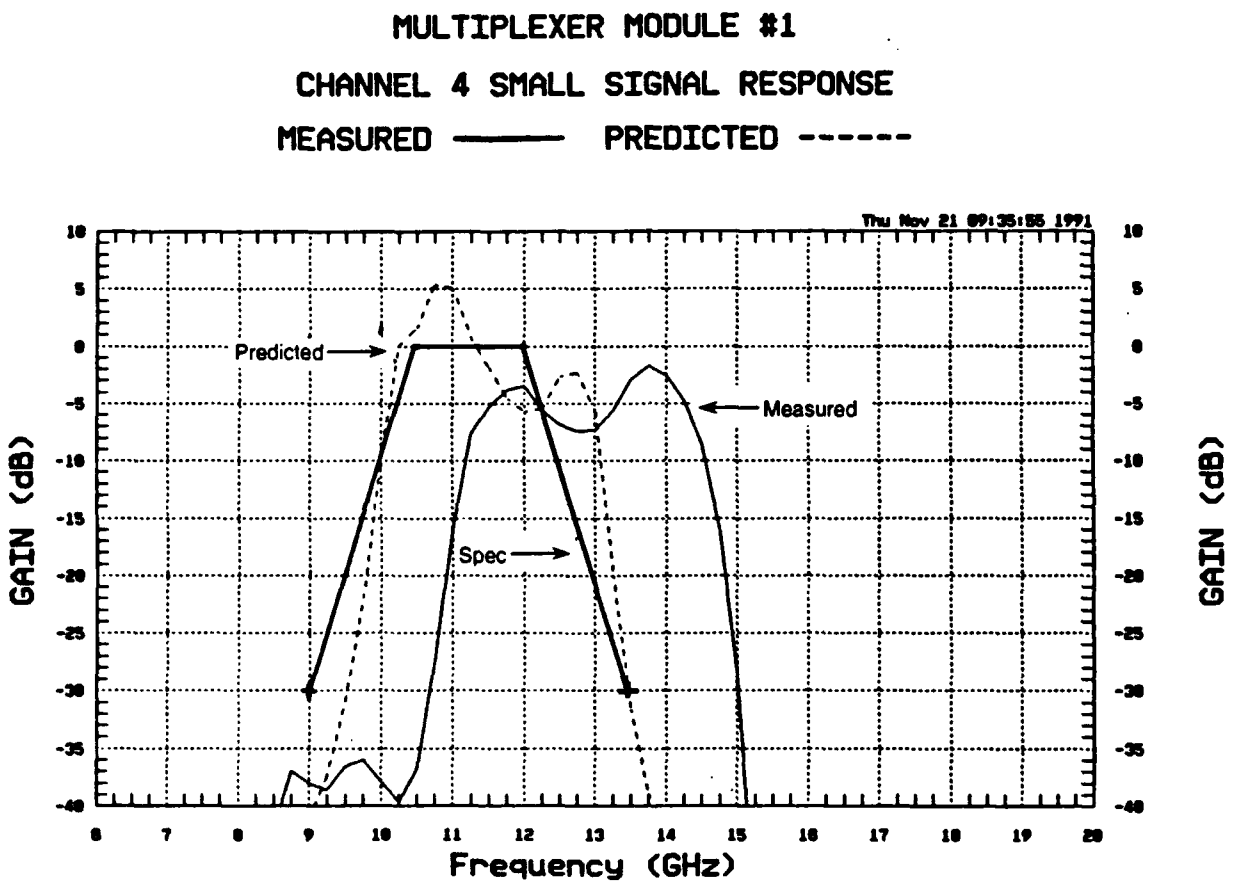


Figure 5-7. Multiplexer Performance, Channel 4 Response.

PBN-91-2627

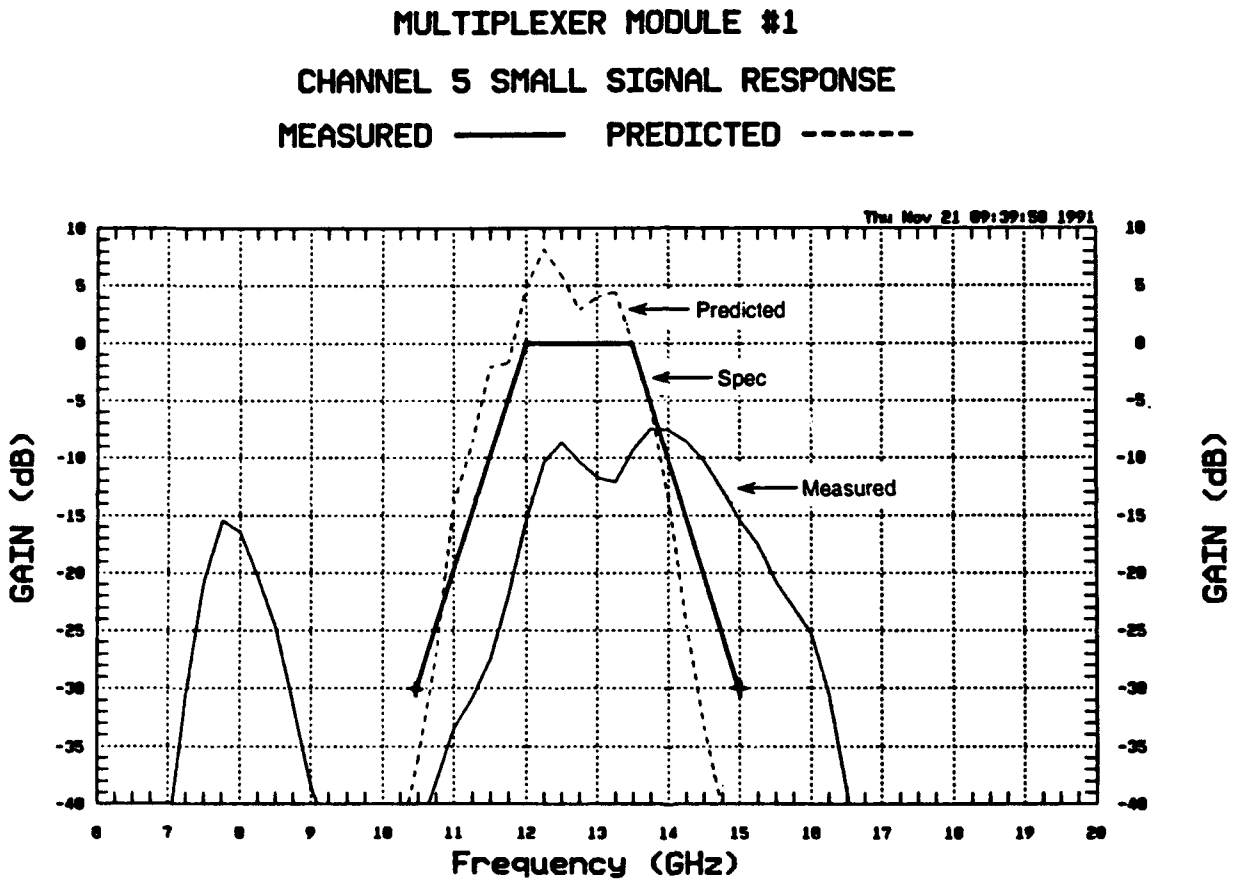


Figure 5-8. Multiplexer Performance, Channel 5 Response.

PBN-91-2628

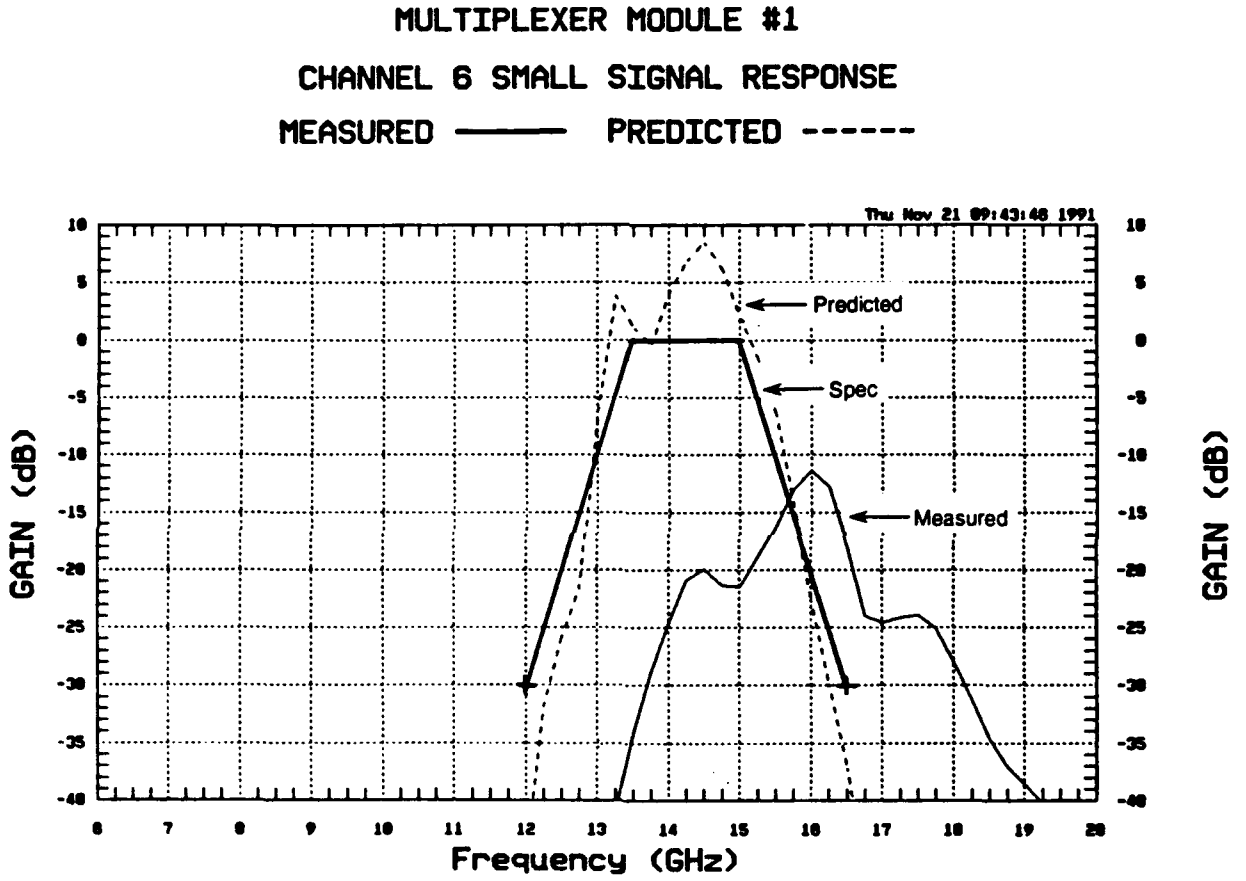


Figure 5-9. Multiplexer Performance, Channel 6 Response.

PBN-91-2629

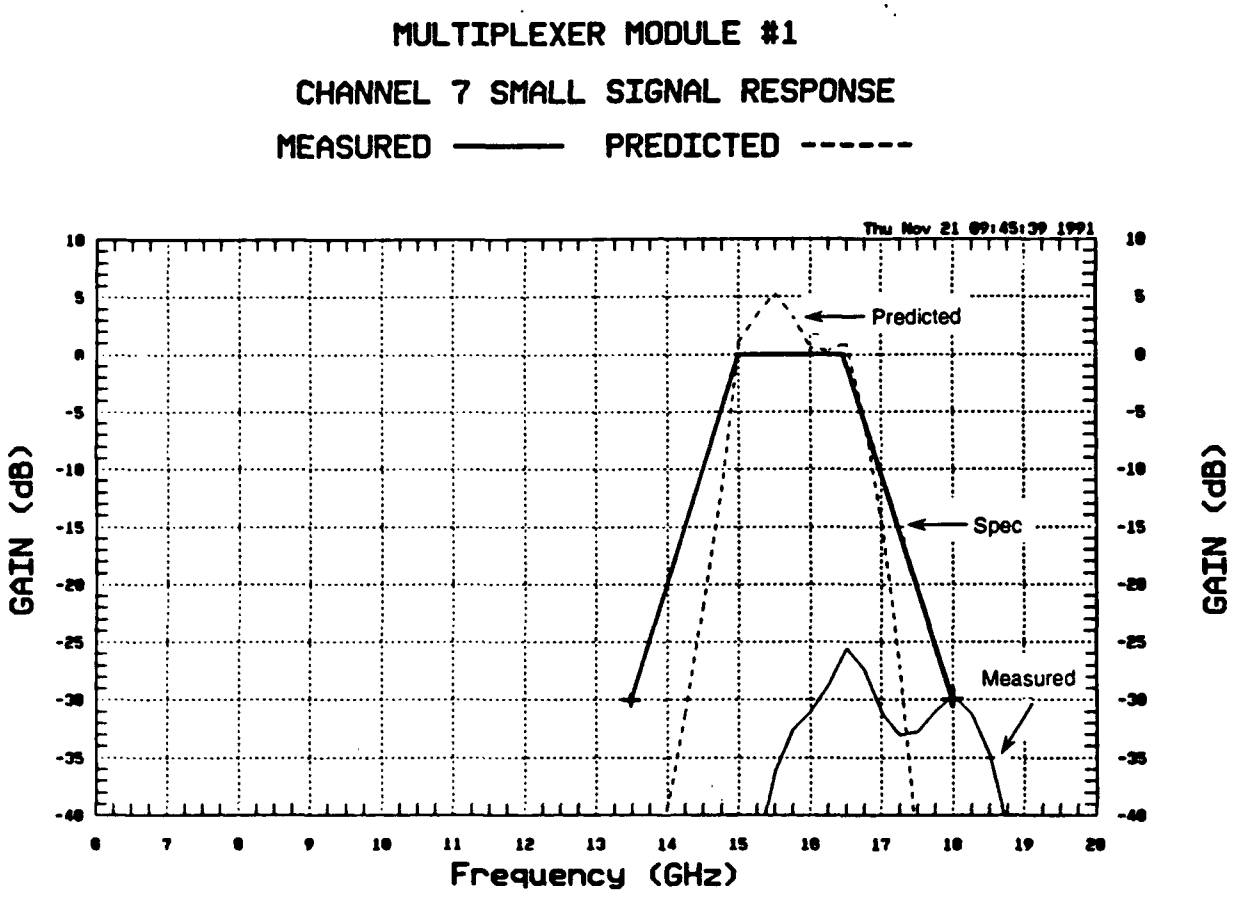


Figure 5-10. Multiplexer Performance, Channel 7 Response.

PBN-91-2630

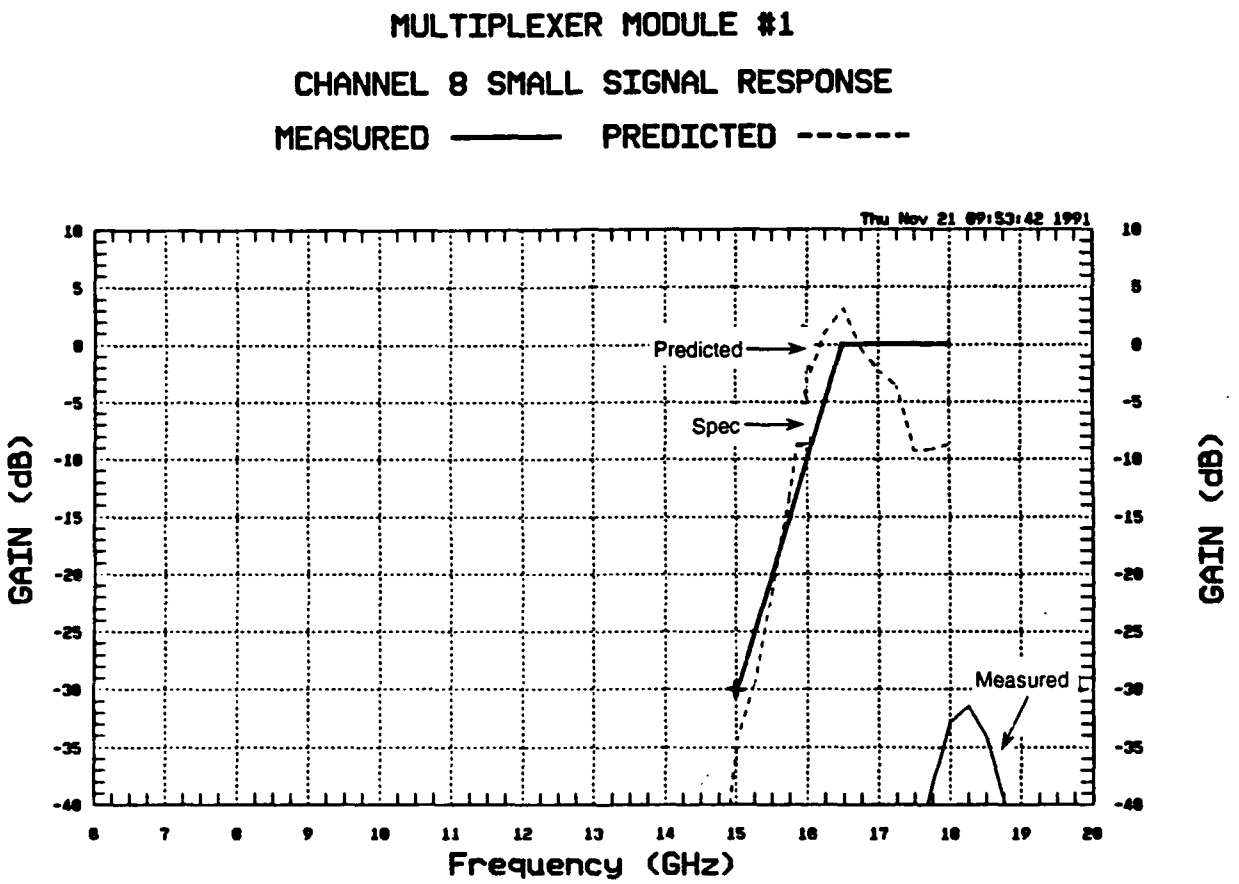


Figure 5-11. Multiplexer Performance, Channel 8 Response.

PBN-91-2631

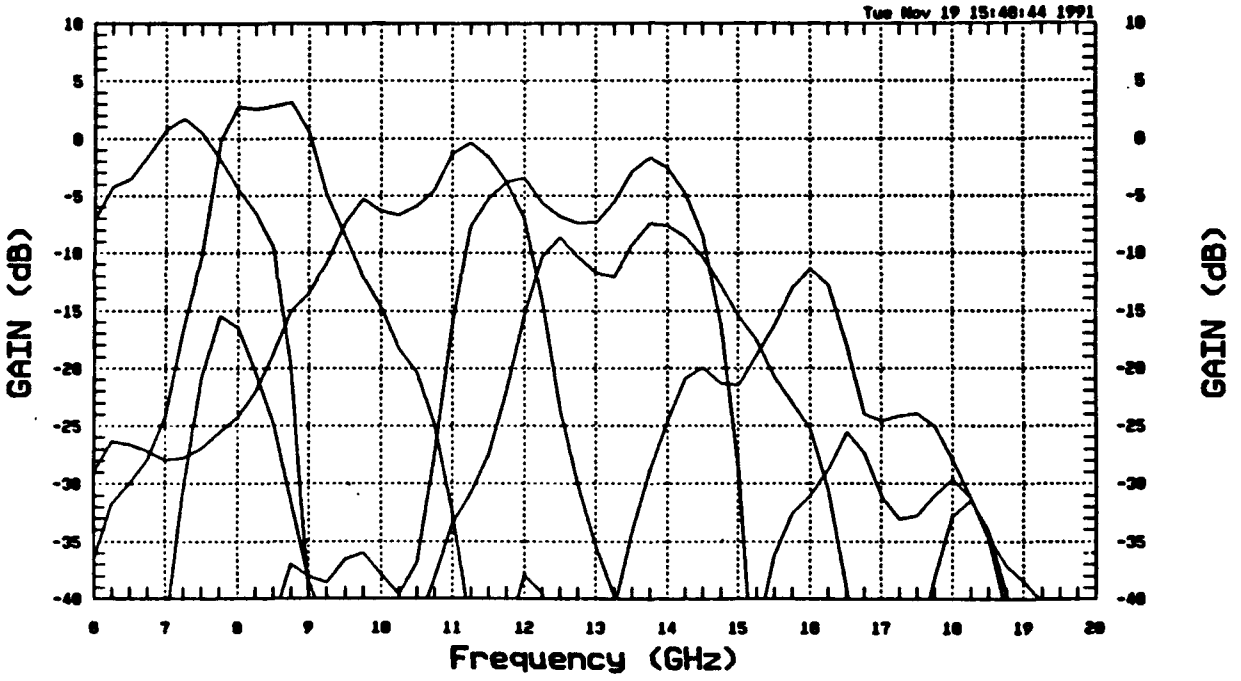


Figure 5-12. Multiplexer Module No. 1 Composite Response.

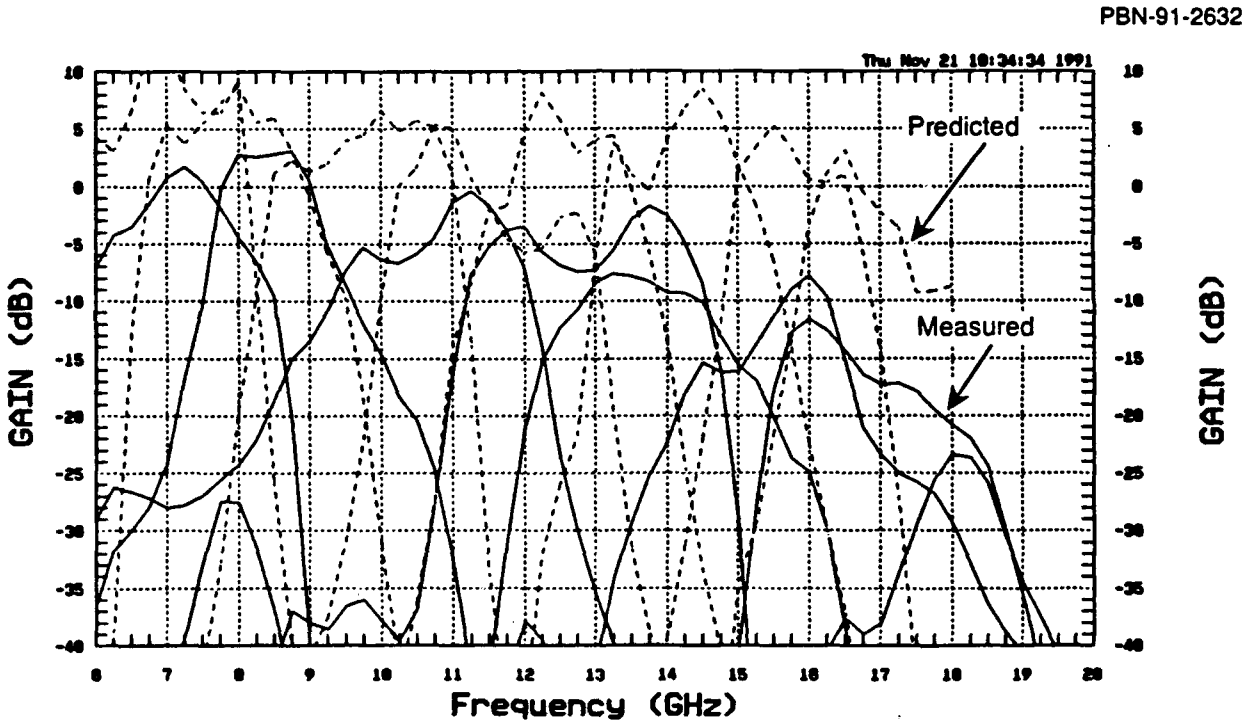


Figure 5-13. Multiplexer Module No. 1 Composite Response, 12 GHz Low Pass Turned Off for Channels 5 through 8.

PBN-91-2633

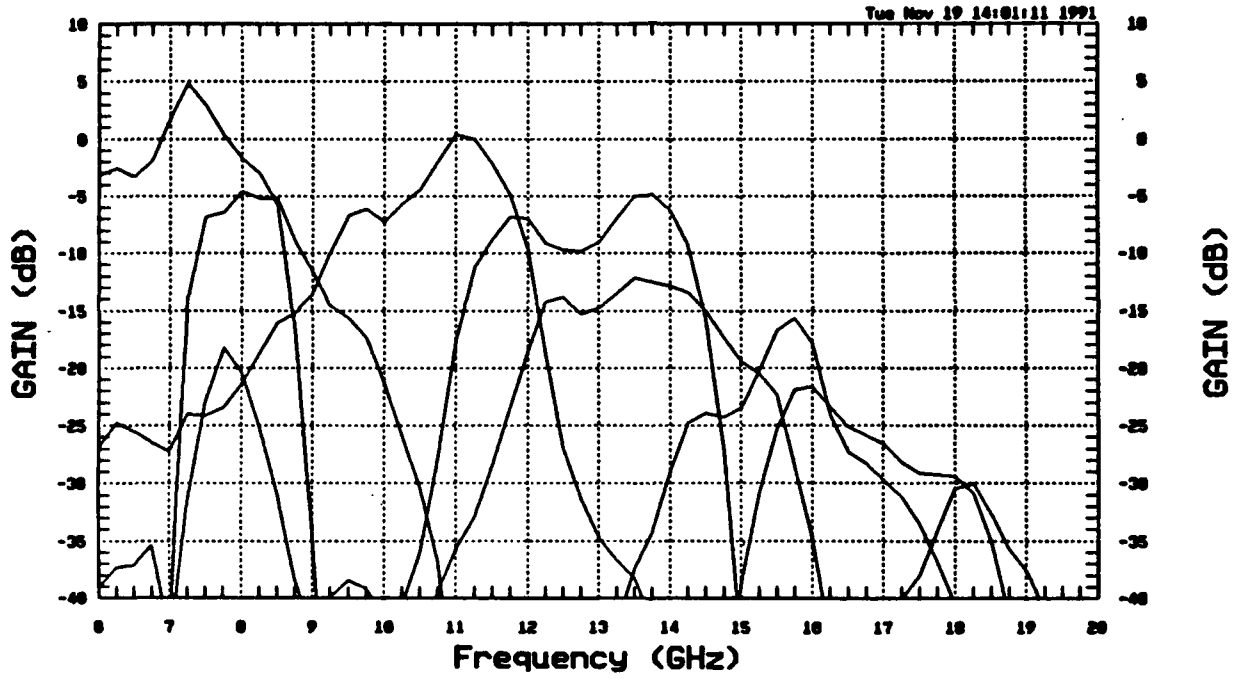


Figure 5-14. Multiplexer Module No. 2 Composite Response.

Gain and noise figure were measured on both delivered modules on channel 4. The results are shown in Figures 5-15 and 5-16. The power output was measured on a 10.5 GHz diplexer at 11.5 GHz and 12 GHz frequencies. The performance is plotted in Figure 5-17.

The data taken on the two delivered modules is analyzed in Section 6.1 and summarized in Table 6-1. The data on each multiplexer channel was taken with all other channels not terminated. The major contribution to the poor performance of some of the channels is believed to be due to the coupling between the transmission lines, capacitor losses, coupling between the transmission lines and components. Because of the limited budget of this program, we were unable to model these effects properly. Degradation in multiplexer performance due to diplexer interactions and mismatch was also predicted.

5.3 Processing

The multiplexer wafers were processed using a standared low noise MMIC process. The FET active layer was formed by ion implantation with a doping level of $4 \times 10^{17} cm^{-3}$. The FET gate length is 0.5 μm. The gates are biased through 2 kΩ resistors and all FET bias circuitry is included on chip. The chips are passivated with 2000 Å of silicon nitride which is also used as the capacitor dielectric. Inductive elements were formed using high impedance transmission lines. Upon completion of front-side processing, the wafer was thinned to 4 mils and 50 μm via holes were etched. Figure 4-3 shows a chip photograph of a typical diplexer chip. Each diplexer chip measures 96 x 146 mils (2.4 x 3.7 mm).

5.4 Multiplexer Performance Summary

Two wideband microwave multiplexer modules were assembled and characterized. Diplexers were used as building blocks in both multiplexer configurations. In order to obtain low pass band loss and high signal rejection out of band, lumped/transversal element filters were used to form the diplexers.

PBN-91-2636

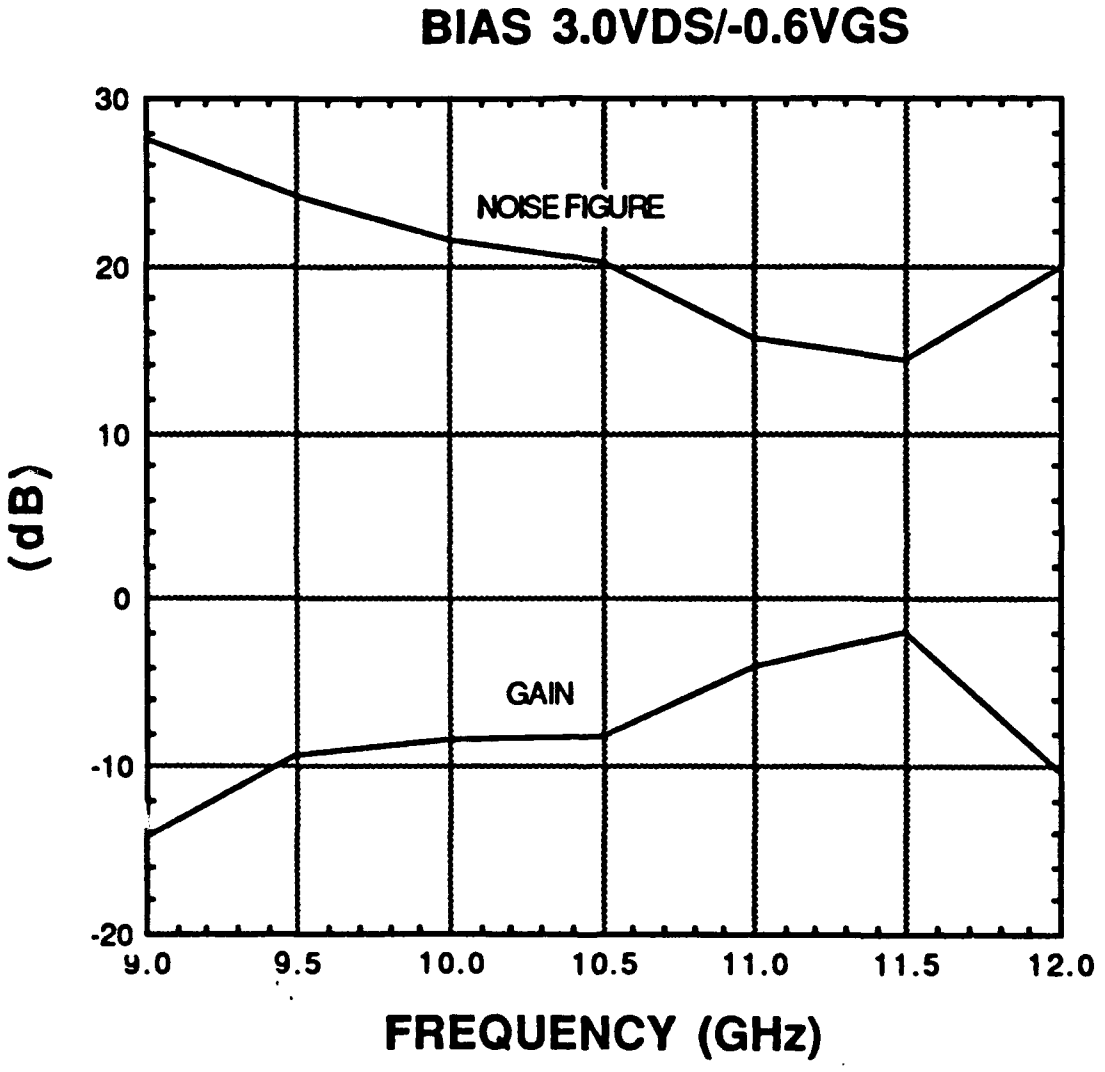


Figure 5-15. Multiplexer Module No. 1 Gain and Noise Figure Performance.

PBN-91-2637

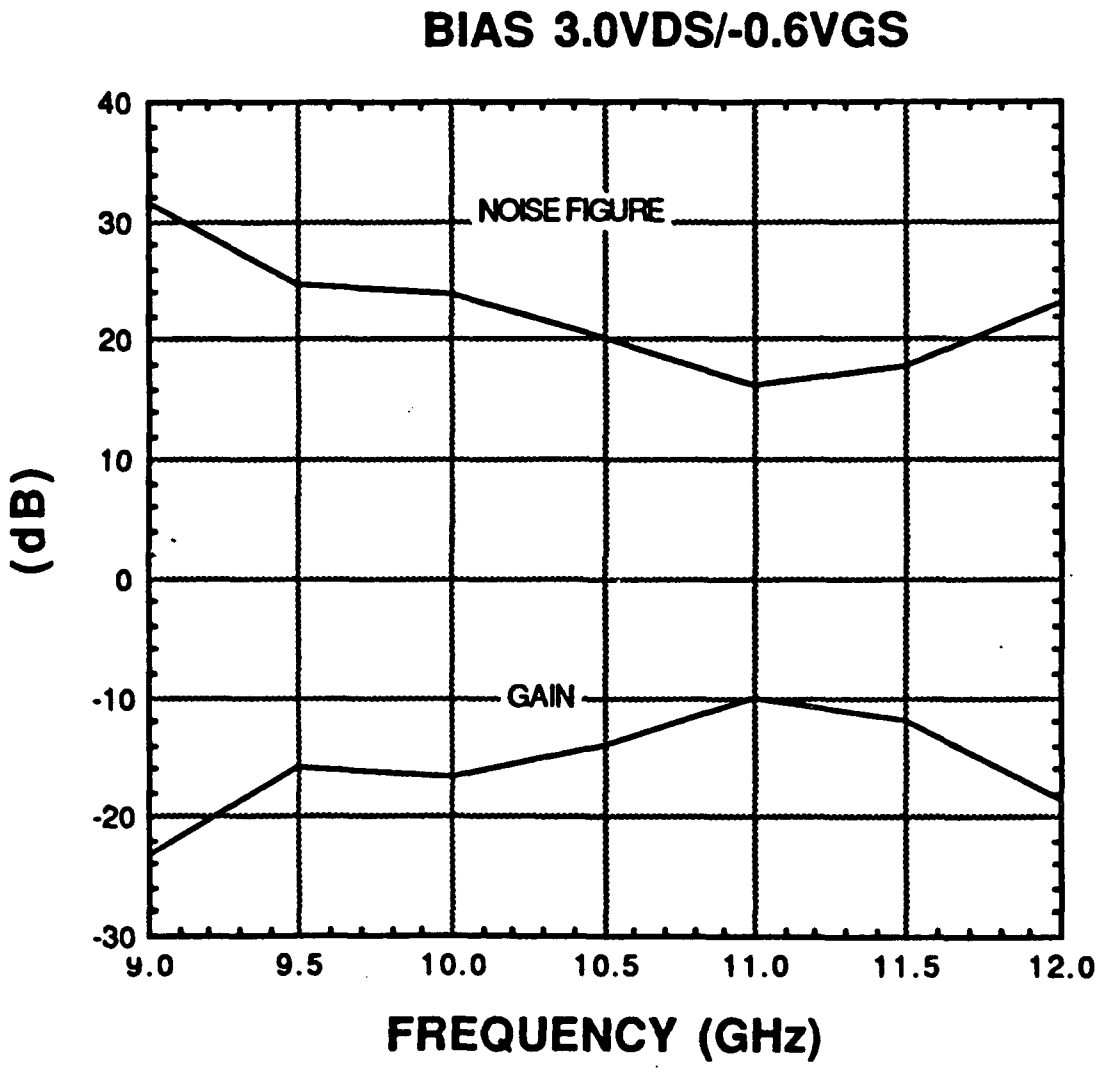


Figure 5-16. Multiplexer Module No. 2 Gain and Noise Figure Performance.

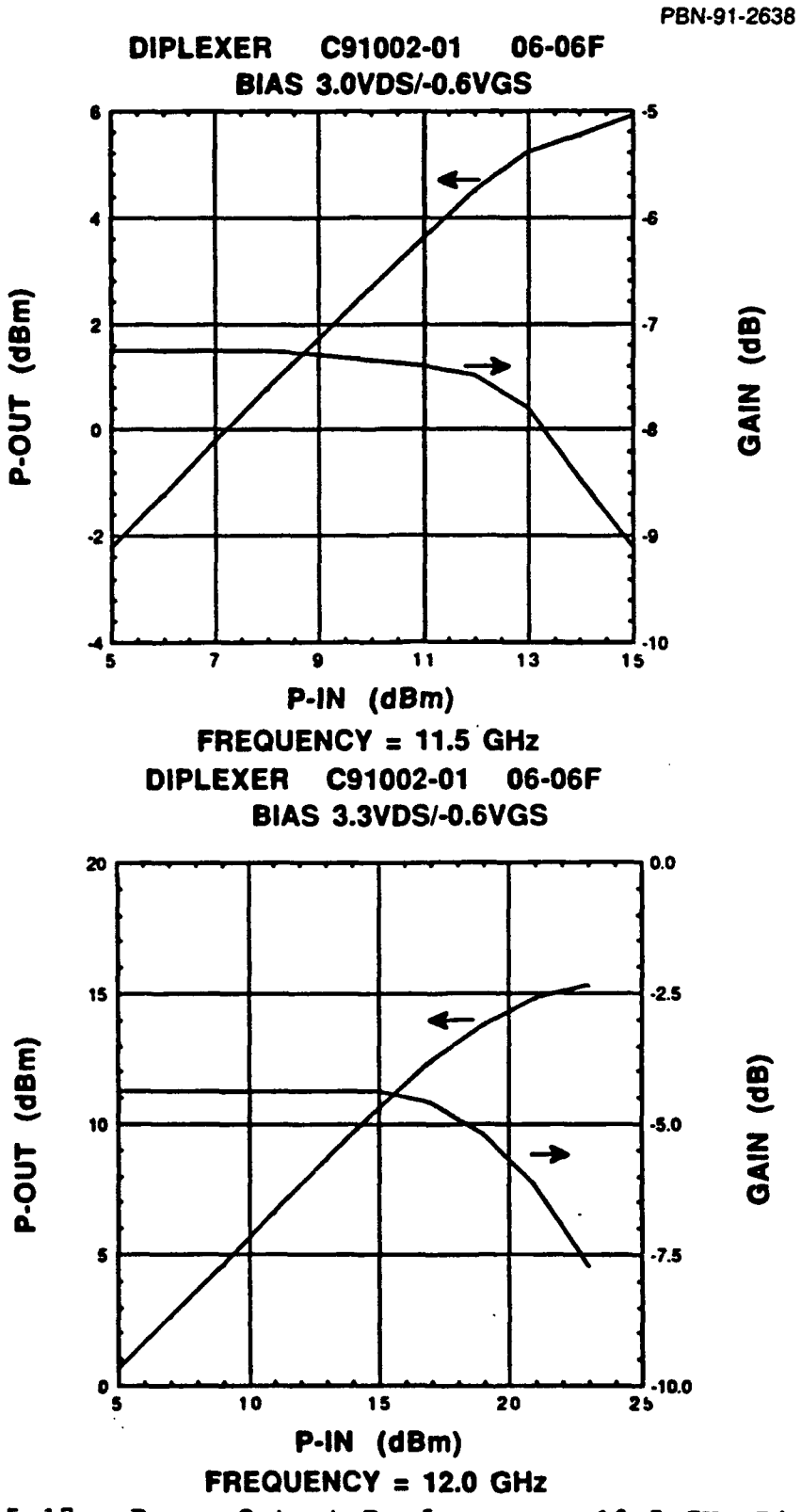


Figure 5-17. Power Output Performance, 10.5 GHz Diplexer.

6.0 CONCLUSION

In Phase 1 of this program, a novel MMIC compatible filter concept was explored, extended to the diplexer case, and successfully demonstrated. In Phase 2 of this program, multiple diplexers were integrated to provide an eight channel multiplexer. Although not all goals could be met within the limits of this program, with additional effort all of the program goals could be met.

The sections below provide detailed analysis of our multiplexer approach and its limitations, and a discussion of actual system requirements and how they can best be addressed. In Section 6.1, the performance of the completed multiplexers is summarized and compared to the original goals. Methods of meeting all goals are also described. (Causes of major performance deficiencies are also discussed in Section 5.) In Section 6.2, a generic system application is presented and the compatibility of this and other multiplexer approaches is discussed in light of the performance attributes of other system components.

6.1 Multiplexer Performance

The performance achieved with the two complete and delivered multiplexers under this program is summarized in Table 6-1. The original program goals are also listed. The two complete multiplexers did not meet all goals, but generally, goals were met for some sub-bands, or at some frequencies. This is sufficient to show that most goals could have been met, and that the approach is viable. In the paragraphs below, the performance deficiencies for each goal are summarized and analyzed. An approach to achieving each goal is also provided.

Table 6-1
Multiplexer Performance Summary

	Program Goal	Unit 1	Unit 2
Frequency Band	6 to 18 GHz	6 to 18 GHz	6 to 18 GHz
Sub-bands	8 almost equal	8 ≃ equal	8 ≃ equal
Gain	0 dB	+3 to -25 dB	+5 to -25 dB
Rejection 1.5 GHz from Sub-band Edge	30 dB	20 to 40 dB	20 to 40 dB
Noise Figure	12 dB	14 to 20 dB*	16 to 22 dB*
1 dB Comps. Power	15 dB	5 to 13 dBm**	4 to 13 dBm**
IP3 (input)	not specified	20.3 dBm*	19.9 dBm*

* measured in the 10-11.5 GHz sub-band
** measurements made on component diplexers

6.1.1 Sub-Bands

The program objective was to achieve 8 equal sub-bands across the 6-18 GHz band. Some of the sub-bands were shifted in frequency, were narrower or were broader than desired. These deficiencies are all caused by frequency shifting in the component diplexers. The filter approach we selected can support a wide range of sub-band widths, and can be configured to provide virtually any number of sub-bands.

The frequency shifting that occurred in some diplexers is attributable to two effects: one, inadequate design model accuracy, and two interaction between diplexers. The accuracy of the design models was limited by interactions between elements in these relatively complex MMICs, and could not be adequately simulated with conventional microwave CAD (both SUPERCOMPACT® and TOUCHSTONE® were used). Only a single design/process pass was possible within the scope of the program. EM simulation likely can provide more accurate results, but these circuits will not fit into a single simulation, so significant approximations must be made. Further, at the time the

diplexers were in design, EM simulators were not readily available, and such an effort would be beyond the scope of this contract.

The effect of diplexer interactions was expected during the design of the multiplexer. It was a customer decision to forego the additional design effort to compensate for these interactions. In a conventional multiplexer, diplexer interactions are extremely difficult to correct. Our approach, however, affords considerable addition flexibility since only two band edges interact at any single junction. As a result, diplexer interaction can be compensated for in a straightforward, though somewhat laborious process.

6.1.2 Gain

The gain in some sub-bands exceeded the 0 dB goal but, in many, the goal was missed by a significant margin. Measurements of the component diplexers showed that virtually all achieve 0 dB gain in their pass-bands. This not only demonstrates that the gain goal was achievable, but also suggests the cause of the low gain in some multiplexer sub-bands. All multiplexer sub-bands are realized by the cascade of low-pass and high-pass responses from diplexers. When these are shifted towards one another in frequency, the result is very low gain. The 0 dB gain goal is achievable with the selected approach and device (ion implanted MESFET). Higher gain devices are available (such as PsHEMT), and could readily provide 2 to 3 dB additional gain per diplexer, so 6 to 10 dB multiplexer gain would be possible.

6.1.3 Rejection

It has been demonstrated that this approach can yield the required 30 dB rejection. The short fall in some sub-bands is due to modeling inaccuracies and diplexer interactions, as discussed. It would be possible to further improve rejection by adding more elements (both lumped and transversal) at the cost of lower gain. Alternatively, multiple filters can be cascaded, at the cost of higher dc power consumption.

6.1.4 Noise Figure

The principal cause of high noise figure is low (or negative) gain with active devices. At frequencies where gain is high (near 0 dB), the noise figure goal is almost met. This suggests that the noise figure goal could be met if 0 dB gain were achieved across all sub-bands. Further improvements would be possiible with a lower noise device (such as a PsHEMT). The process we used to fabricate the diplexers typically provides 2 dB noise figure at 10 GHz, 3.2 dB at 18 GHz. Our PsHEMT, in contrast, provides 0.6 dB noise figure at 10 GHz, 1.5 dB at 18 GHz. Also important is the fact the PsHEMT offer much lower R_n. The devices in the diplexers are not noise matched: the lower R_n makes the device match much less critical to achieve low noise. Further, since the use of PsHEMTs, would provide 2-3 dB gain per diplexer, the effects of additive noise would be significantly diminished. Noise figure of each diplexer was not measured. A noise figure of 10 dB per diplexer with 0 dB gain yields a 14.7 dB multiplexer noise figure. The use of HEMTs should reduce the noise figure of each diplexer to 6-7 dB. With 2-3 dB gain per diplexer, multiplexer noise figure will be 8-9.5 dB.

6.1.5 Output Power

The output power capability of the multiplexers has been determined by measuring the 1 dB gain compressed power level for two of the component diplexers. The measured 1 dB compressed power, at 5 to 13 dBm, falls short of the 15 dBm goal. For many applications, such a low output power capability is acceptable (so long as IP3 is high enough). Nonetheless, output power can be increased. Since the circuits were operated at 3 V, considerably higher power would be expected at 5-7 V. The cause of the low output power capability is likely the poor power match presented to the large gain device. By reducing the filter terminating resistances from 350 to 750 Ω (as used in our diplexers) to 50 Ω, far better power match could be achieved (at the cost of 3 to 5 dB gain per diplexer). It would therefore be possible to meet the 15 dBm power goal, with an upper limit of 20 dBm. This would be at the cost of reduced gain and increased power consumption.

6.1.6 Intermodulation Distortion

We have used the Third Order Intercept point (IP3) to characterize Third Order Intermodulation Distortion (IMD) at low signal levels. The 20 dBm input IP3 was measured for both multiplexers. As discussed below, systems typically require much higher IP3. The devices used in this program (ion implanted MEFSFETS) have modest linearity. Should PsHEMT, be used in their place, gain and noise figure will improve, but IP3 will degrade. PsHEMTs are relatively non-linear, worse than ion implanted MESFETs (see Table 6-2). The device option with the most promise for higher IP3 is a spike-doped MESFET. As seen in Table 6-2, this device is ten times more linear than a PsHEMT. The gain and noise that can be achieved simultaneously with high IP3 is, however, no better than that of an ion implanted MESFET. There is, therefore, a device choice that must be made, PsHEMT for high gain and low noise, or spike MESFET for IP3. The development of a device wl ich simultaneously provides low noise and high IP3 would be ideal, for this application and numerous others.

Table 6-2
Comparison of Key Device Attributes at 10 GHz
for Candidate Low Noise Devices

Device Type	P_{1dB}	IP3	$IP3/P_{dc}$	NF
Spike-Doped PsMESFET	16.5 dBm	42 dBm	84	1.8 dB
Spike-Doped MESFET	18.0 dBm	42 dBm	50	1.9 dB
Single Pulse PsHEMT	12.5 dBm	23 dBm	1.6	0.6 dB
Ion-Implanted MESFET *	14 dBm	30 dBm	12.6	1.8 dB

* Device type used in the multiplexers demonstrated under this program

The circuit configuration used in the diplexers is not well-suited to achieving high IP3. Small FETs (the transversal elements) are exposed to substantial relative RF levels, resulting in significant distortion. It is possible to increase the size of the transversal elements as long as their gain is reduced. Even with the use of a spike-doped MESFET, input IP3 of no more than 35 dBm can be expected of a complete multiplexer.

6.2 System Needs

A typical broadband (6 to 18 GHz) receive system configuration is illustrated in Figure 6-1. The LNA is as near the front-end as possible in order to set the system noise figure. Phase shifters and attenuators follow along with gain blocks (referred to as post amplifiers) which make up the remaining system gain. Typically, a wideband system is divided into several sub-bands before mixing down to the IF frequency. This frequency multiplexing function allows continuous surveillance of the entire band to be maintained with reasonable IF frequencies.

One of the major limitations of a broadband system such as the one in Figure 6-1 is its vulnerability to jamming. Any signals within the 6 to 18 GHz band can intermodulate with one another and generate numerous false tones. A possible solution is to place the multiplexer up front, reducing the bandwidths within which intermodulation can occur. As was indicated in Section 6-1, however, a multiplexer with simultaneous low noise and high IP3 cannot presently be achieved with our approach. In fact, no other multiplexer provides both low noise and high IP3 either. Because of this limitation, the multiplexer cannot presently be placed up front.

As is shown in Figure 6-2, tunable filtering at the front end is also an attractive option. For EW applications, a tunable bandstop filter is preferred (to block out a jammer). For radar applications, a tunable bandpass filter is preferred (to block out all signals except the desired one). Low noise figure is an

important requirement, since the filter(s) would be at the front end. There is no available tunable filter technology that can provide these functions with sufficiently low noise. Ferrite approaches, now under development, may provide adequate performance.

The problem with jamming and intermodulation can be significantly diminished if the LNA is very linear. If so, the LNA will generate few intermodulation products, and filtering can be achieved after the LNA with relaxed noise figure requirements. As was indicated in Table 6-2, an ultralinear device has been demonstrated. (This work is being performed under a separate NRL Contract, No. N00014-89-C-2136.) Such an approach is illustrated in Figure 6-3. In this case, the filters must have exceptional linearity (IP3 should be at least 35 dBm, 45 dBm for many applications). Active tunable filters cannot, generally, provide adequate IP3.

The multiplexer can also be placed directly after the low distortion LNA. In such a configuration, the multiplexer divides the band into several sub-bands, significantly diminishing the occurrences of intermodulation. This would then allow the IP3 requirements of all following circuits to be relaxed somewhat. The input IP3 of the multiplexer, however, must still be quite high. The 35 dBm achievable with our approach must be considered a minimum, a 45 dBm input IP3 would be preferred.

6.3 Summary

In this program, a novel filtering concept was studied, and successfully adapted to diplexers. MMIC diplexers were successfully demonstrated. A full family of MMIC diplexers was developed and integrated as a functional multiplexer. Although not all program goals were met, it was shown that the goals all can be met. Our ability to do so was primarily limited by the small budget available to this effort. In summary, this has been an extremely successful program, and has demonstrated that a level of performance compatible with system requirements can be achieved.

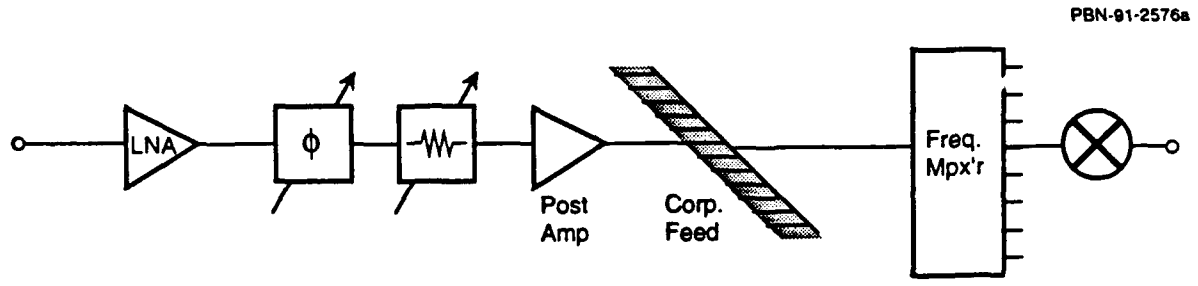


Figure 6-1. Block Diagram of a Generic Wideband Receiver.

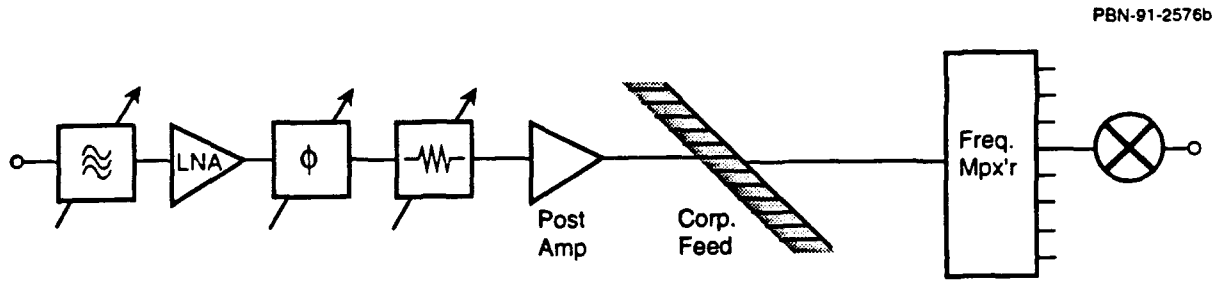


Figure 6-2. A Wideband Receiver with Tunable Filtering at the Front End. The tunable filter must have very low noise.

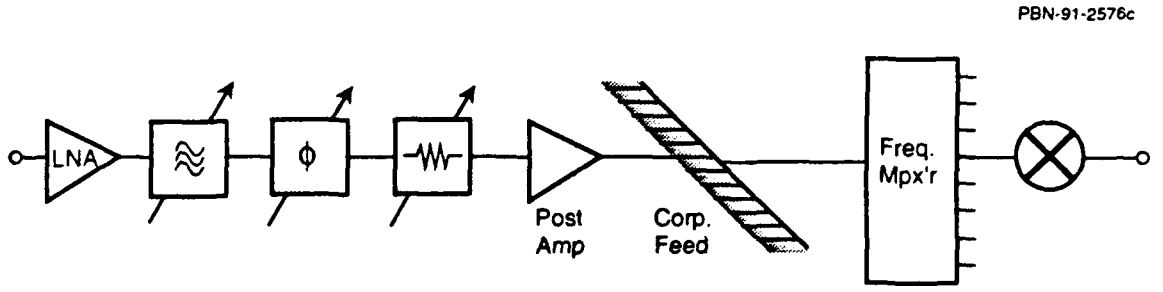


Figure 6-3. A Wideband Receiver with Tunable Filtering After the LNA. The noise requirement on the filter is relaxed, but both the LNA and filter must have very high IP3.

APPENDIX A

A NOVEL MMIC ACTIVE FILTER WITH LUMPED AND TRANSVERSAL ELEMENT

M-4636a

A Novel MMIC Active Filter with Lumped and Transversal Elements

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A novel active filter structure has been developed and demonstrated as an MMIC. This filter structure makes use of both lumped elements and active transversal elements. The combination of lumped and transversal elements provides performance superior to that of a filter made of lumped elements alone, and is much smaller than a filter made of transversal elements alone. This miniature MMIC filter has a pass band of 9.8-11.1 GHz with 2 dB loss, and better than 30 dB rejection 1.1 GHz from either passband edge. This level of performance could not have been achieved on a conventional 4 mil thick GaAs MMIC with only passive lumped elements.

I. INTRODUCTION

Microwave filters are generally realized with networks of distributed elements that can be quite large, or with discrete lumped elements which require custom tuning. For many applications, the size of distributed element filters is excessive. The cost of lumped element filters can be prohibitive. MMIC filters would offer the possibility of both small size and low cost.

The development of MMIC filters has received little emphasis, and the limited results that have been achieved have been disappointing. In general, MMIC filters are made with lumped capacitors and inductor equivalents (spiral inductors and/or high impedance transmission lines). MMIC filters are typically only used where they are required as part of another function which is implemented on MMIC [1]. This is primarily attributable to the poor performance that may be expected of conventional MMIC filters.

Inductor equivalents on MMICs are of relatively poor performance, regardless of whether they are spirals or high impedance line sections. They suffer from both low Q and low self reso-

nant frequency. Spiral inductors typically have a Q of 30 at 10 GHz. Self resonant frequency varies with inductor size; the largest value inductor that can practically be made with a self resonant frequency below 18 GHz is on the order of 2 nH. Because of these limitations in inductor performance, filters with sharp cut-off characteristics cannot be realized. Somewhat better performance may be achieved if the substrate is thicker than the conventional 4 mils. Nonetheless, adequate filter response is generally unachievable.

The use of MMIC compatible transversal and recursive filters has been reported. The size of a conventional transversal filter is excessive for a pure MMIC implementation. This has been circumvented by using an off chip delay line [2]. The size of the complete filter assembly is still quite large. Novel topologies of transversal and recursive filters have also been shown [3]. These filters are smaller than conventional implementations, and could conceivably be implemented as MMICs, although very large ones. An MMIC transversal filter implementation of a vector modulator has been demonstrated [4]. Since the objective was to achieve varying phase and amplitude, rather than filtering, a small monolithic realization was possible.

The filter reported in this paper uses lumped elements to achieve a basic band pass filter response. Active transversal elements are used to sharpen the band pass characteristic, and to overcome the high loss of MMIC lumped elements. Inductors have been realized with high impedance transmission lines; spiral inductors may be substituted without significant effect on performance.

II. CIRCUIT APPROACH

A typical microwave transversal filter structure is shown in figure 1. In such a filter, multiple amplitude elements (transversal elements) are combined 180° out of phase. The phase delay is provided by 90° line lengths on the input and output sides [5][6]. The outputs of the amplitude elements add constructively or destructively, depending on frequency. By appropriate selection of the number of transversal elements, and by tailoring their amplitudes, a wide range of pass band characteristics may be realized. Because of the nature of this filter approach, parasitic (harmonic) pass bands are present. Generally, a large number of transversal elements are required to achieve reasonable filter response. On the order of 25 transversal elements and 12.5 wavelengths of transmission line would be required in order to achieve the same level of performance as is demonstrated by the filter presented in this paper. The size of a such a filter would be inappropriate for MMIC implementation.

The filter presented in this paper utilizes both transversal and lumped element filtering. Lumped filter elements provide basic band pass response. Transversal elements are also used. The constructive and destructive addition of multiple signals is used to enhance the filter characteristic.

The lumped element portion of the filter is shown in figure 2. A conventional low pass filter is used on the input. This is followed by a gain element, and then by a conventional high pass filter. The characteristic of this filter is that of a conventional lumped element band pass filter, with some added gain. The phase characteristics of this circuit may, however, be used to advantage.

The low pass filter may be thought of as a delay line. For a single delay line section, as in figure 3(a), the ratio of input to output voltages is:

$$\frac{V_1}{V_2} = \sqrt{1 - \omega^2 LC}\left[\sqrt{1 - \omega^2 LC} + j\omega\sqrt{LC}\right] \tag{1}$$

For $\omega^2 LC \leq 1$, this relationship may be rewritten as:

$$\frac{V_1}{V_2} = (1 - \omega^2 LC) + j\omega\sqrt{LC(1 - \omega^2 LC)} \tag{2}$$

It can be seen that a cut-off frequency may be defined as $\omega_c = 1/\sqrt{LC}$ and that the phase relationship between the input and output voltages of the low pass section may be written as:

$$\theta_{lp} = \sin^{-1}(\omega\sqrt{LC}) \tag{3}$$

This phase relationship has been plotted over normalized frequency in figure 4. As can be seen, phase delay is small at low frequency, and approaches 90° as cut-off is approached.

Similar calculations can be done for the high pass section in figure 3(b), which may be thought of as a phase advance line. The ratio of input to output voltages is:

$$\frac{V_1}{V_2} = \sqrt{1 - \frac{1}{\omega^2 LC}}\left[\sqrt{1 - \frac{1}{\omega^2 LC}} + \frac{1}{j\omega\sqrt{LC}}\right] \tag{4}$$

For $\omega^2LC \geq 1$, this relationship may be rewritten as:

$$\frac{V_1}{V_2} = \left(1 - \frac{1}{\omega^2 LC}\right) - j\sqrt{\frac{1}{\omega LC}\left(1 - \frac{1}{\omega^2 LC}\right)} \qquad (5)$$

It can be seen that a cut-off frequency may once again be defined as $\omega_c = 1/\sqrt{LC}$, and that the phase relationship between the input and output voltages of the low pass section may be written as:

$$\theta_{hp} = \sin^{-1}\left(\frac{1}{\omega\sqrt{LC}}\right) \qquad (6)$$

This phase relationship has been plotted over normalized frequency in figure 5. As can be seen, phase delay is negative (therefore is a phase advance). It is small at high frequency, and approaches -90° as cut-off is approached.

The filter approach presented in this paper takes advantage of the combined phase delay of high pass and low pass sections. As an example, a low pass section and a high pass section have been designed. The low pass section consists of a 0.5 nH inductor and a 0.2 pF capacitor, and has a cut-off frequency of 15.9 GHz. The high pass section consists of a 0.3 pF capacitor and a 0.75 nH inductor, and has a cut-off of 10.6 GHz. The sum of the insertion phase (positive phase advances and negative phase delay) of these sections is plotted in figure 6. At 13 GHz (the middle of the frequency band between the upper and lower cut-offs) total insertion phase is 0 degrees. Insertion phase deviates significantly from 0 degrees as either cut-off frequency is approached. This frequency dependent phase deviation is utilized to achieve transversal filtering in the filter presented in this paper.

The block diagram of the complete lumped and transversal element filter is shown in figure 7. The main signal path is through the last gain element, A_n. Lower amplitude gain elements are used for A_1 through A_{n-1}. Each gain element (A_x) has an insertion phase from input to output ($\emptyset_x$) for its signal contribution. It is the deviation of any insertion phase element ($\emptyset_x$) from the insertion phase of the main signal path ($\emptyset_n$) that allows transversal filtering to take place. Wherever the difference between $\emptyset_x$ and $\emptyset_n$ is 180° or near 180°, substantial signal amplitude reduction is possible. This is similar to conventional transversal filtering. The difference in phase increases as either cut-off is approached (see figure 6), therefore transversal filtering can readily be utilized to enhance the cut-off characteristics of the lumped element filter.

Since the basic filter pass band characteristic is determined by lumped elements, very few transversal elements are required to produce a filter with sharp cut-off characteristics. Further, the transversal elements are relied on to achieve the sharp cut-off characteristics, therefore low Q lumped elements can be tolerated.

III. DESIGN EXAMPLE

The schematic of the demonstrated band pass filter is shown in figure 8. The basic structure of figure 7 is used. This filter could accommodate up to five transversal elements, even though only three are needed to achieve adequate performance.

The design procedure begins with the design of the lumped element low pass and high pass filters. Conventional nine element Chebychev filters are used for each. The low pass filter is designed for the desired upper pass band cut-off, the high pass filter is designed for the desired lower pass band cut-off. The two filters are cascaded through a single FET. Since this FET is in the signal path it determines filter gain. In order to maximize gain, it is desirable to maximize the periphery of the FET. The periphery of this FET is limited by the last shunt capacitor in the input low pass filter. Since the FET has considerable gate capacitance, the FET is sized so that its gate capacitance replaces the last shunt capacitor. Note that the first shunt inductor in the output high pass filter must be adjusted to compensate for the drain capacitance of the FET. Also note that the both the low pass and high pass filters are terminated by a 50 Ω resistor. This ensures both that the lumped element filters are properly matched. Further, it ensures the stability of the FET over a very wide frequency range. This completes the design of the lumped element portion of the filter. The filter, as is, provides a reasonable band pass filter filter characteristic, although without sharp cut-off skirts.

The design of the transversal elements can proceed, given the guidelines of section II above. In order to demonstrate the potential for transversal filtering, the insertion phases of the the signal paths through FET1, FET2 and FET3 were determined (using conventional modeling software). Since the main signal path ($\emptyset_3$) is through FET3, it is most revealing to express the phases of the other signal paths relative to $\emptyset_3$. Figure 9 shows the insertion phase difference for FET2 ($\emptyset_3$-$\emptyset_2$) and for FET1 ($\emptyset_3$-$\emptyset_1$). It is apparent that the signal path through FET1 can offer complete signal cancellation near 8.5 GHz at the lower cut-off, and near 11.25 GHz at the higher cut-off. Similarly, the path through FET2 offers complete cancellation near 12.25 GHz at the high end cut-off, and partial cancellation over the 7-8 GHz band at the lower cut-off (since 180° phase difference is not fully achieved).

The predicted performance for the filter is summarized in figure 10. Three curves are shown, one (labeled FET3 only) shows the filter with no transversal elements, one (labeled FETs 2 & 3) with partial transversal elements, and the last (labeled FETs 1, 2 & 3) for the complete filter with all elements. When no transversal elements are used, conventional band pass filter performance is expected. This is the case represented in figure 2. When the transversal elements are added, the band edge rejection skirts are sharpened considerably. Note that the transversal elements limit ultimate filter rejection (far from the band edges), in return for improvements in rejection on the skirts. In the case of the filter presented in this paper, a 30 dB ultimate rejection goal was used.

IV. MMIC FABRICATION

The filter was fabricated as an MMIC and is shown in figure 11. Inductive elements are implemented with high impedance transmission line sections. The capacitors are made with a 2000 Å silicon nitride dielectric. The transversal elements are standard low current, ion implanted FETs with 0.5 μm gates and 3×10^{17} cm^{-3} doping. All bias circuitry is included on chip. Each FET has a drain bias circuit, implemented through the shunt inductors of the high pass filter. The drain biases are tied together on chip, but since the connections are made through airbridges, they are readily separated. This is useful for performance diagnosis, and is not generally used. The gates are individually biased through 2 kΩ resistors, although they are generally biased by a common voltage. The wafer was thinned to 4 mils and 20 x 100 μm vias holes were etched. The complete MMIC measures 70 x 75 mils (1.8 x 1.9 mm), including some area taken up by optional test patterns. Chip size could be further reduced by removing the test patterns and replacing some high impedance line sections with spiral inductors.

V. MEASURED PERFORMANCE

The measured performance of the filter is shown in figure 12. Passband loss is 2 dB, with 1 dB ripple. For a strictly passive lumped element filter, the passband loss would be on the order of 9 dB. The active transversal elements reduce the loss by approximately 7 dB. Greater than 30 dB rejection is achieved 1.0 GHz from the lower passband edge, 1.1 GHz from the upper passband edge. Modeling shows that with a conventional lumped element filter such rejection could at best have been achieved 2.2 GHz from the passband edges. Return loss is 5 dB or better with-

in the passband, and approaches 0 db outside of the passband, as would be expected from a lumped element filter. The FETs in the filter are biased at 3 volts on the drain, and -0.8 volts on the all gates (~40% I_{dss}). Performance is essentially unaffected over a drain voltage range of 2.5 to 7 volts. Current consumption is 42 ma, so at 3 volts, power consumption is only 126 mW.

In order to confirm the contributions of the transversal elements, separate biases were provided to each FET, allowing each of their gains to be removed. This was done by reducing drain bias to 0 volts, and gate voltage to beyond pinch-off (-4 volts). This allows the most of the effect of any given FET to be removed, but since a substantial capacitive path still exists from gate to drain (~0.3 pf/mm), the effect of any FET could not be completely removed. The results of this experiment are shown in figure 13. The curve labeled "all FETs" is the same as S_{21} in figure 11. The other two curves indicate the performance when FET1 is turned off, and when both FETs 1 and 2 are turned off. FETs 1 and 2 do not contribute much gain, so the pass band loss does not change significantly. Note that the cut off frequencies are not significantly changed when FET1 and FET2 are turned off, but near in rejection degrades substantially.

Figure 13 shows measured performance curves which may be directly compared to the predicted curves in figure 10. The major difference between the measured and predicted curves is a shift in the pass band of approximately 0.5 GHz, indicating errors in the models of some of the lumped elements. The pass band shape, the rejection shape, and filter rejection are all modeled quite accurately. The effect of the transversal elements is confirmed in the measurements, even though it is not possible to fully remove the transversal elements.

VI. SUMMARY

A novel filter structure has been described using a combination of lumped and transversal elements. The resulting filter yields performance superior to that which can be achieved with lumped elements alone, and in a much smaller size than could be realized with transversal elements alone. A 9.8-11.1 GHz MMIC band pass filter was designed and fabricated to demonstrate the concept.

Although only a passband filter was shown, the concept can readily be extended to include low pass filters, high pass filters, and diplexers. Similar circuitry can be envisioned to include recursive elements.

ACKNOWLEDGEMENT

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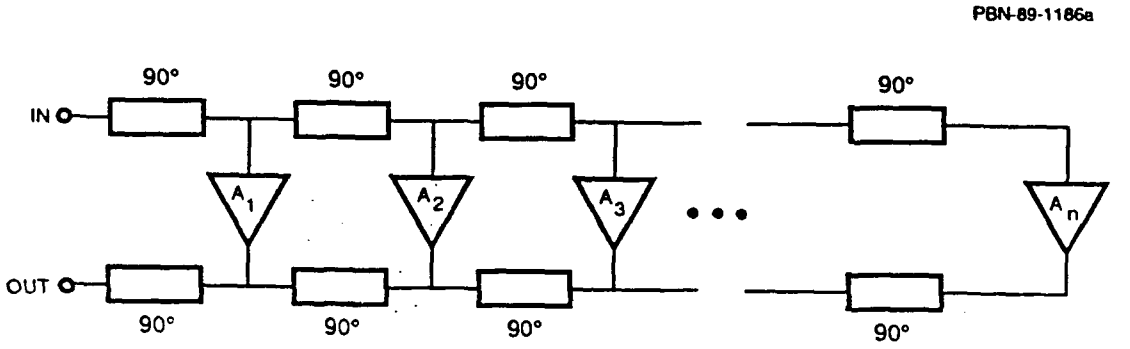


Figure 1. Conventional microwave transversal filter structure.

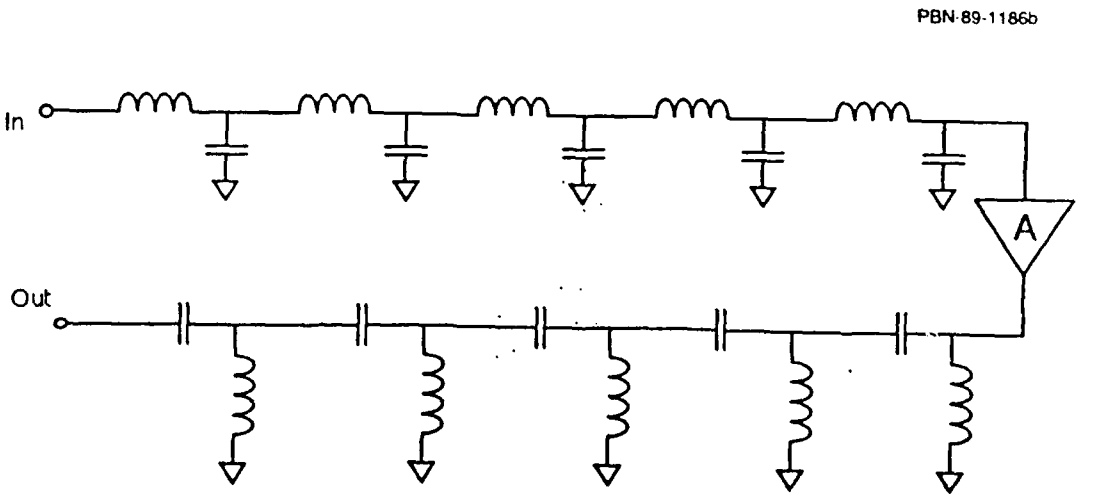
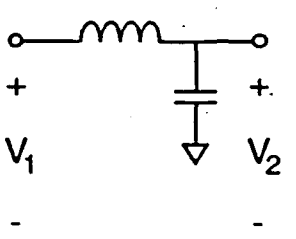


Figure 2. The lumped element portion of the filter, consisting of a low pass filter, an active gain element, and a high pass filter in cascade.



(a)

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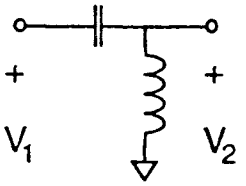

(b)

Figure 3. Single section (a) delay line, (b) advance line.

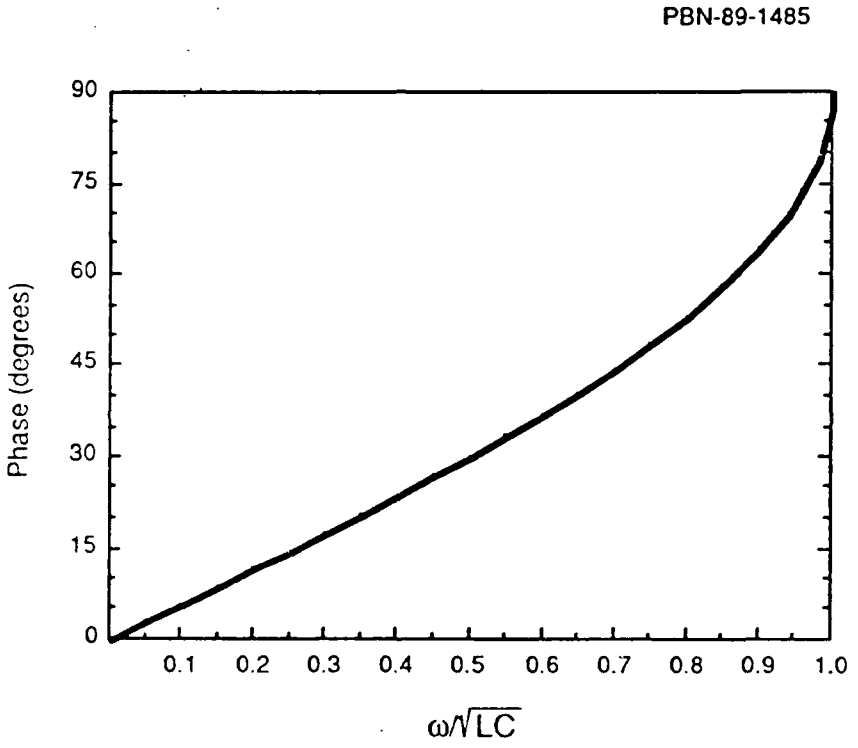

Figure 4. Phase characteristic of a single section delay line.

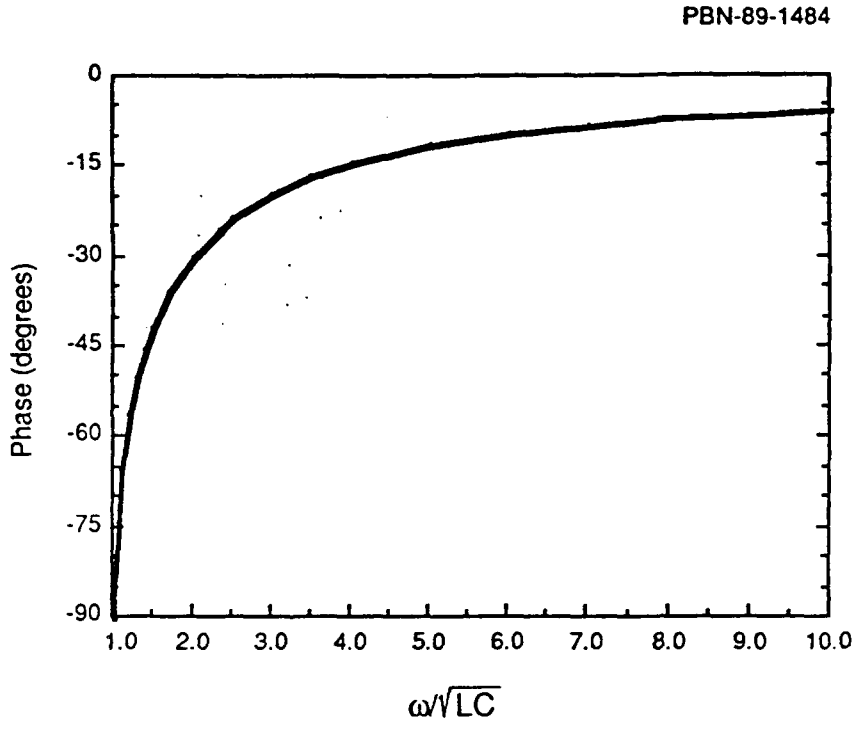

Figure 5. Phase characteristic of a single section advance line.

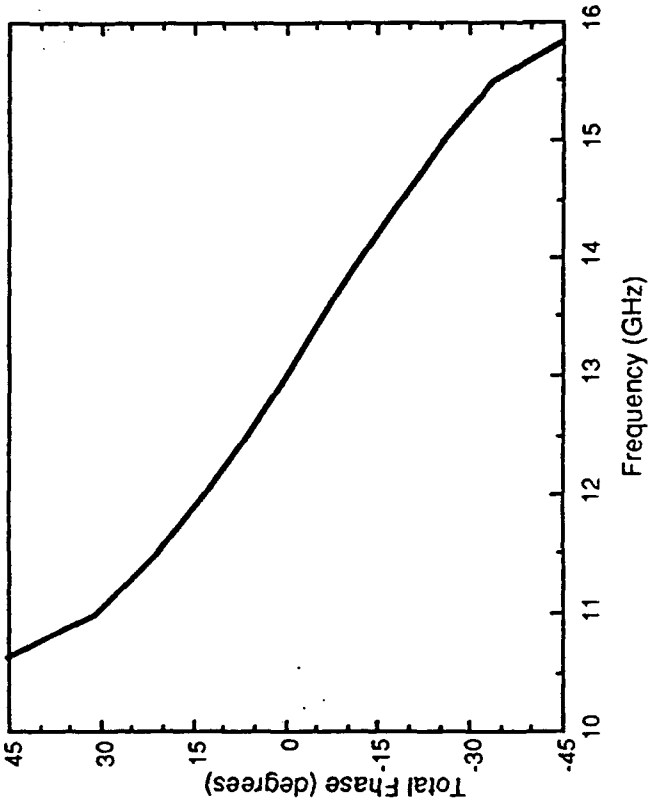

Figure 6. Phase characteristic of the single section delay line plus single section advance line example.

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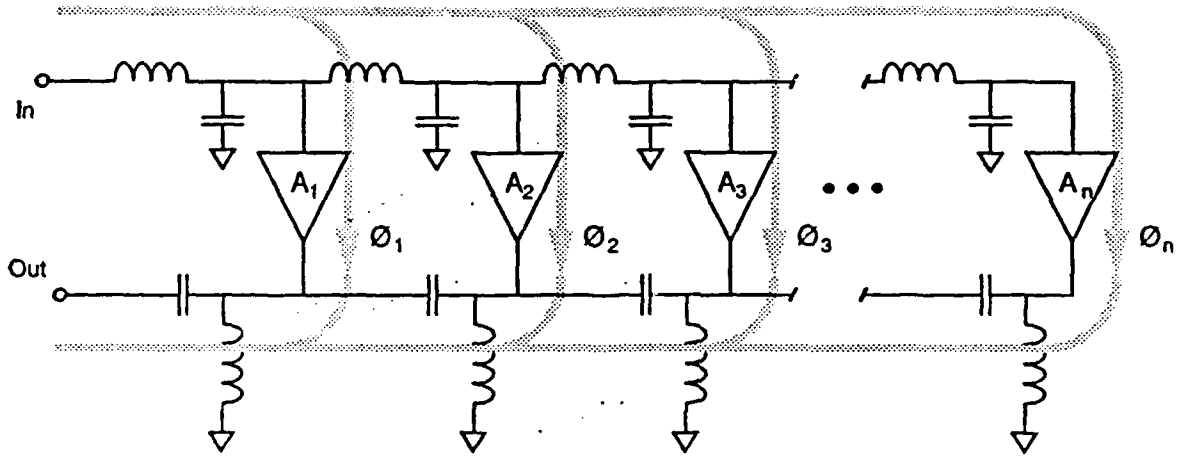

Figure 7. Structure of a lumped and transversal element filter.

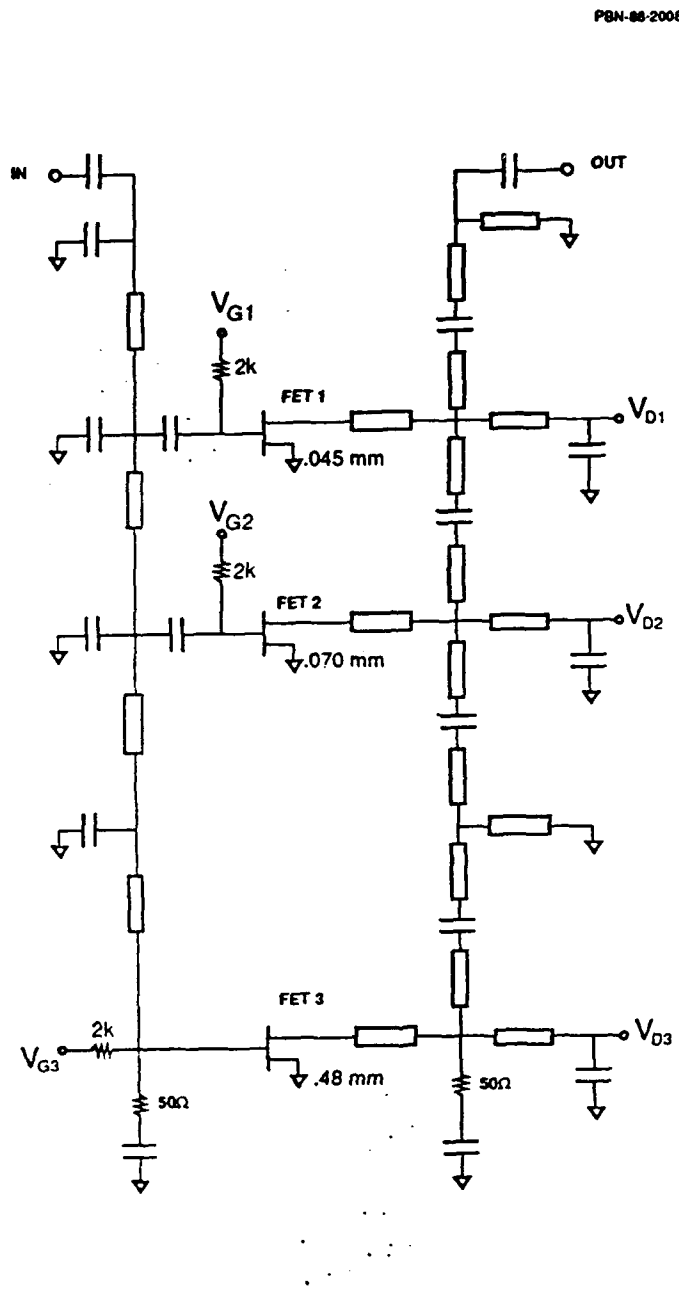

Figure 8. Schematic for the lumped and transversal element band pass filter example.

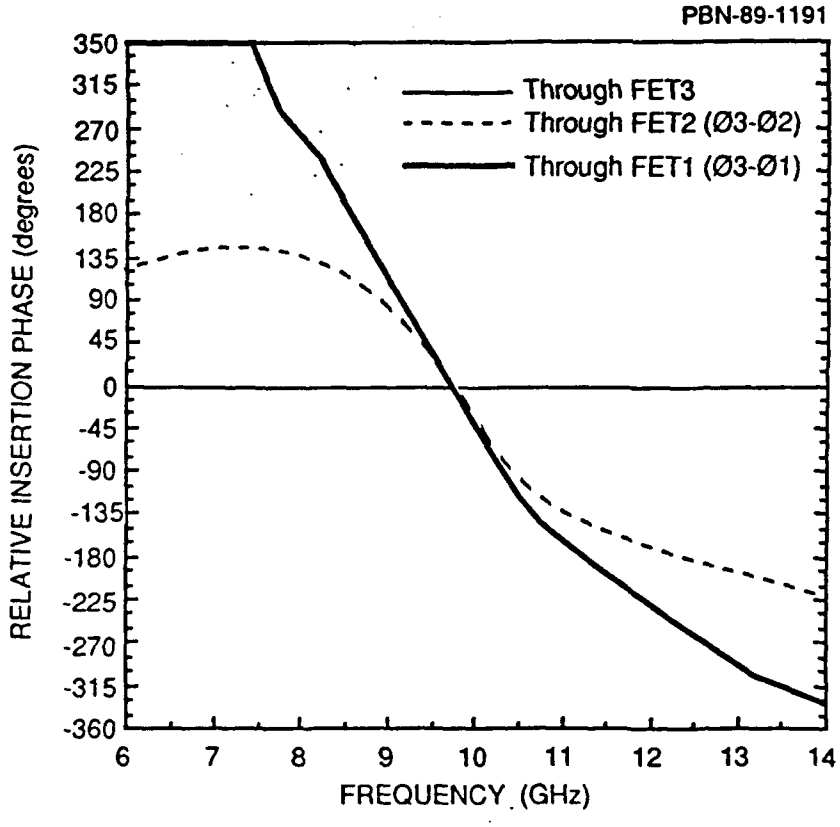

Figure 9. Relative insertion phases through each FET of the lumped and transversal band pass filter example.

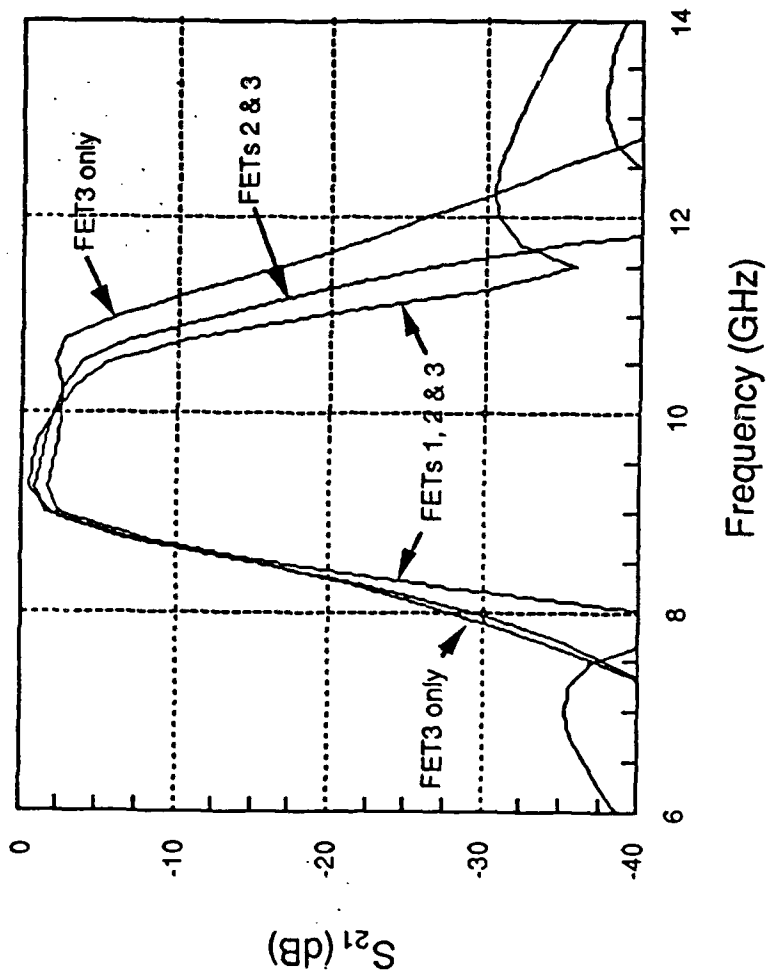

Figure 10. Predicted band pass characteristics of the filter example with all, some, and no transversal elements.

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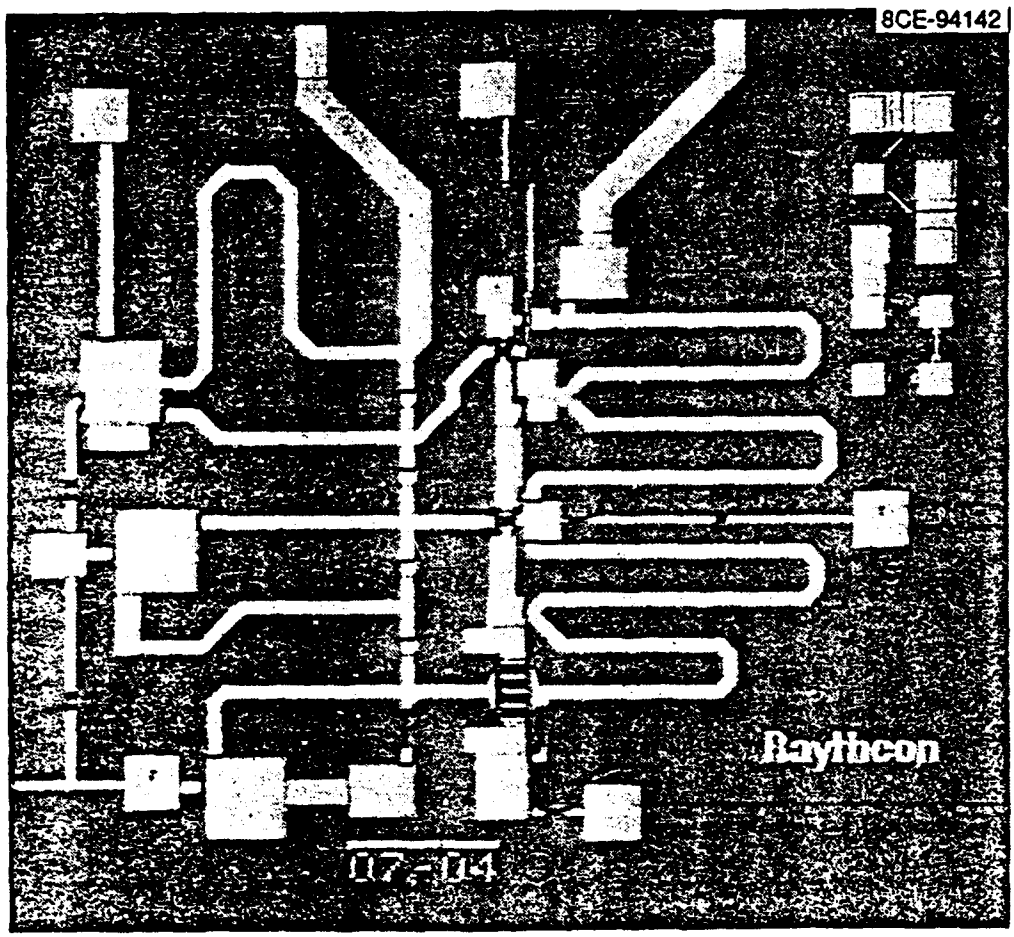

Figure 11. Photograph of the 9.8-11.1 GHz band pass filter MMIC.

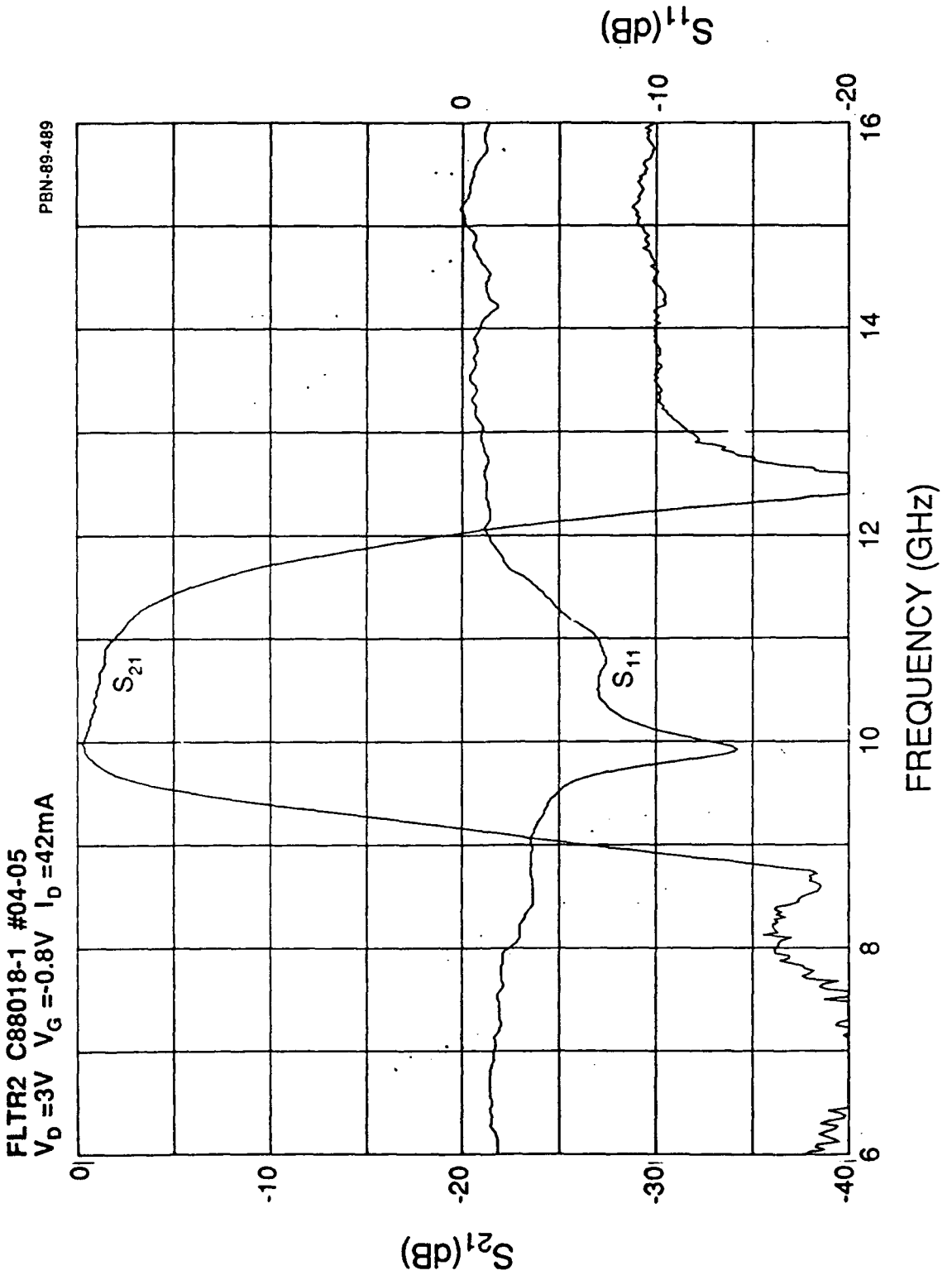

Figure 12. Measured performance of the 9.8-11.1 GHz band pass filter MMIC.

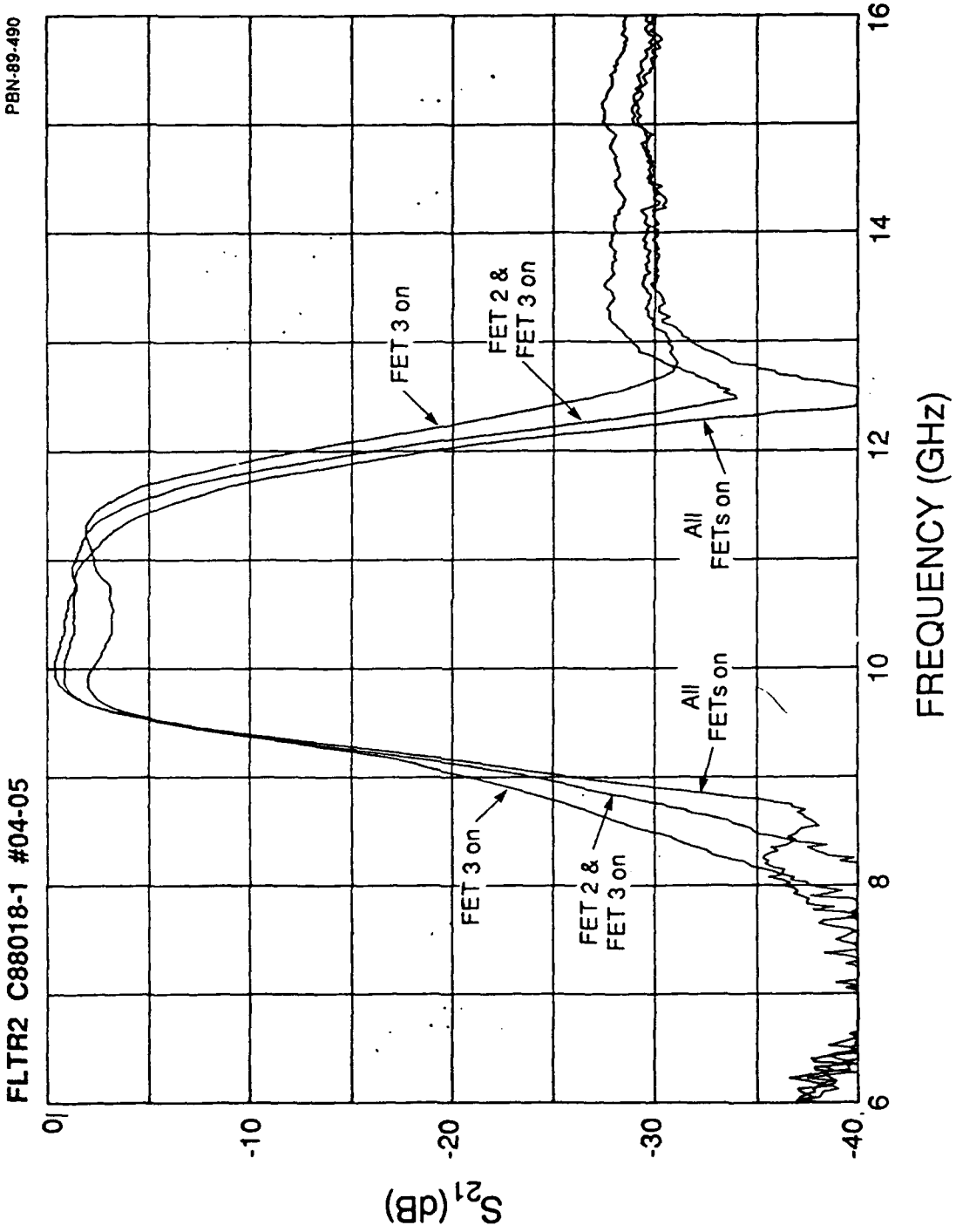

Figure 13. Measured performance of the 9.9-11.1 GHz band pass filter in normal operation, and when some FETs are turned off.